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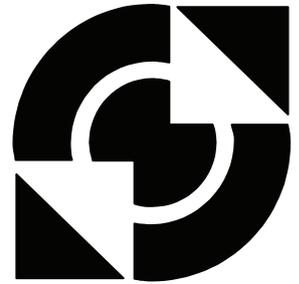
Faculty of Electrical Engineering, Mathematics & Computer Science

Switched Mode Piezo-Panel Driver

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Abstract

The subject of this thesis is the design of a system which can drive piezo-panels. This system is called the piezo driver. The piezo-panels are used for an *Active Noise Cancelling* (*ANC*) system which is being developed to be used inside the cabin of airplanes. The piezo driver fills the gap between the calculating system, which provides the anti-noise signal, and the piezo-panel.
The total ANC system is designed as one complete system. The piezo driver has to be placed on the panel and therefore the piezo driver is integrated on chip.
Further the undesired electric behaviour of the piezo-panel is not allowed to affect the output signal. The piezo driver is designed to drive piezo elements in the specified range of 50 nF to 500 nF.

Piezoelectric material shows hysteresis between the applied voltage and the displacement of the material. Besides this, the material also shows resonance behaviour. For low frequencies the piezoelectric material behaves like a capacitor. The material requires high driving voltages.
Studies show that the hysteresis can be solved by applying charge control. The resonance behaviour can be predicted with the use of a model. This model uses the mechanical and electric properties of the piezo-panel to do so. The electric impedance of the piezo element can also be simulated with the help of the model.

The main function of the piezo driver is to amplify the input signal. Because of the high driving voltages, dissipation is an issue. Research of several amplifier stages shows that a class-D topology will give the lowest dissipation.
The class-D design is adjusted to the electric behaviour of the piezo-panel. The modulator, output filter and feedback of the amplifier design are adjusted for this purpose.

The piezo driver has an analog input and output signal and therefore a PWM modulator is chosen. The reference signal for the PWM modulator is a triangle waveform because this type of waveform will give the best results concerning EMI.
Research of the piezo element shows that for high frequencies the resonance behaviour is very small and can be neglected. The frequency of the triangle waveform is therefore chosen at 1 MHz to have little influence of the piezoelectric resonance.

The output filter used in a class-D design is a *LC* low pass filter. The capacitive behaviour of the piezo element makes it possible to incorporate the piezo-panel into the filter.
The choice of the inductor introduces a problem. The size of the coil is limited because of the maximum thickness of the panel. The maximum available inductor which fits on the panel is used in the filter. The bandwidth is increased by this but does not give any real problems.

Feedback is applied in the piezo driver to improve the quality of the output signal, it reduces noise and distortion. A charge control circuit is implemented into the feedback to control the charge inside the piezo-patch. This reduces the hysteresis effect of the piezo element. The gain in the feedback loop is increased by a loop amplifier. Higher loop gain decreases the effect of noise and distortion on the output signal.

The total functional design is tested and shows good results. The hysteresis and resonance behaviour of the piezo element has little influence on the functionality and output signal of the piezo driver.

The piezo driver design is translated to a circuit design which can be integrated on chip. All the main functions are designed. These are; input buffer, subtractor, PWM modulator and gate driver. The sub-functions are simulated and show good results.

The final piezo driver design is simulated and tested to check the design. Because of the duration of the simulations not all tests have been done with the complete piezo driver design. Simulation of the piezo driver with a non-linear piezo circuit model shows that the charge control works correctly. The requirements are almost all satisfied. The minimum value in the piezo element range forms a problem for the stability of the piezo driver. To ensure stability for this situation some alterations have to be made.

A total circuit design of the piezo driver has been made and simulated. The tests indicate that except for one point all requirements have been satisfied.

Preface

In the course of the last 8 months the author of this report was engaged in his graduation (master's) project. This report is a result of this project. Early July 2006 the author started his research on the piezo driver. Along the way many obstacles were taken. Problems were solved and in the end a final result could be formed.

The subject of this assignment is the piezo driver which comes from TNO's active noise cancelling (ANC) project. TNO is currently working on an active noise cancelling system which can be used in aircraft. The piezo driver is used to drive the piezo-panels. This report describes the research and design of this piezo driver. It took quite some time and effort but the end result is a working design which functions in agreement with the requirements.

The author of this report likes to thank his supervisors at the University of Twente: Ronan van der Zee for his guidance during this project and time for discussion. Arthur Berkhoff for his inside information about the TNO ANC system and the materials he provided. Professor Bram Nauta for his valuable time and suggestions during this project.
The author also likes to thank his parents and girl friend for their support and encouragement throughout the graduation project.

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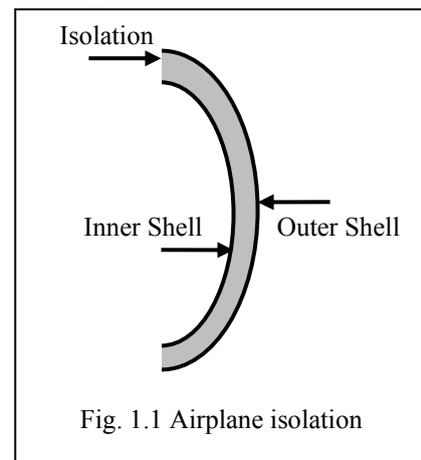
1. Problem definition

This chapter gives an introduction and discusses the assignment of this Master project. The system requirements and demands will be given and also the different parts of the assignment will be discussed. A short definition of the assignment would be:

"Design a system which can drive piezo-panels used for the active noise cancelling system of TNO."

The next part of the problem definition will introduce the assignment. After the introduction the ANC system of TNO is discussed to get a better understanding of the problems and requirements concerning this project. At the end of this chapter a small summary of the assignment and requirements will be given.
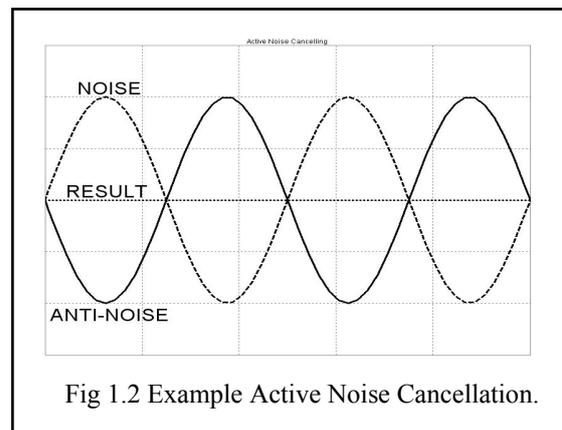
1.1 Introduction

Noise reduction is a point of interest in the aircraft industry. Jet engines produce lots of noise. Passengers like to travel as comfortable as possible in a quiet environment. To reduce the noise inside an aircraft thick isolation is used between the inner and outer shell of an aircraft, see figure (1.1). This passive way of noise reduction does solve the problem but airline companies aren't satisfied. The thick isolation takes up space and weights to much. This leads to less carrying capacity of the aircraft and thus less profit for the airline companies. There is also an active way to reduce noise. This technique is called *Active Noise Cancellation* or short ANC. With ANC a noise-cancellation speaker emits a sound wave with the same amplitude and the opposite polarity to the original sound (noise). These waves combine to form a new wave and effectively neutralize each other out. This is illustrated in figure (1.2).

The improvement of ANC compared to passive isolation is that an ANC system can be made very flat and thus save space and weight. TNO is working on an ANC system

Fig. 1.1 Airplane isolation

which can replace a part of the passive isolation in airplanes but with the use of piezo-panels. The plates are used to generate the anti-noise sound waves. TNO developed a model to predict the vibrations of the panel. This TNO signal system can create a proper anti-noise signal for the piezo-panels and has been designed by TNO. However it needs a bulky amplifier to generate the voltage and current needed. Another system has to be designed which is small enough and is able to drive the patches in a good way.

The design and research of a piezo driver is the subject of this thesis. Before this system can be designed a good understanding of the behaviour of the piezo-panel is needed. The research of the behaviour of the piezo-panel is also presented in this thesis.

Fig 1.2 Example Active Noise Cancellation.

In the following the plate with the piezo-patches will be referred as *piezo-panel*. The system which TNO designed to calculate the correct anti-noise signal will be called *TNO signal system, TSS*. The system which drives the piezo actuators on the piezo-panel is named *piezo driver*. The assignment of this Master project focuses on the research and the design of the Piezo Driver System.

The composition of the report will be as follows. The assignment is split up into several tasks. Each of these tasks is discussed in one of the following chapters. The introduction and problem definition are given in this chapter.

Chapter two discusses the theory and modelling of the piezo-panel. The piezo materials electrical and mechanical properties will be reviewed. The theory is then used to form a model to predict the electrical behaviour of the piezo-panel.

Chapter three is used to find a functional design for the piezo driver. Different functional designs and the several design choices will be discussed. The system requirements and piezo-electric behaviour are used to find the best system design for the piezo driver. The end result of this chapter will be a functional design which is capable of driving the piezo-panels according to the specifications.

In the next chapter, the functional blocks of the design are translated to schematics which can be integrated on chip. Chapter four discusses the several transistor circuit designs, their function and the design choices.

Chapter five is used for the simulation of the piezo driver system. The functionality of the system will be checked. The piezo driver has to satisfy several requirements, this also verified in this section.

The last chapter discusses the conclusion of the assignment and the recommendations.

In the appendixes the several calculations and circuit designs are given. Most circuit design figures are enlarged for a better view.

1.2 ANC system

To understand the place of the piezo driver system within the ANC system, the complete ANC system is discussed here.
The ANC system makes use of a plate with both sensors and actuators attached to it. The whole device, the plate plus sensors and actuators, is referred as piezo-panel. Besides the piezo-panel the ANC system will use the TNO signal system and the piezo driver. The block diagram of the system is shown in figure (1.3).

The sensors on the plate convert the vibrations of the plate to an electric signal. This signal contains information about the vibrations and is used as the input signal for the TNO signal system. The TNO signal system interprets the vibrations and calculates a signal which is used for cancelling the vibrations. This anti-vibrate signal has to be applied to the actuators at the same moment that the vibrations of the plate occur. To sense and counter the vibration at the same time the ANC system has to be in theory infinitely fast.

Fig. 1.3 Block diagram of ANC system

This is in practice of course not possible. TNO developed a model to predict the vibrations of the panel based on the measured vibrations. This prediction model works well for low frequent noise. Noise with higher frequencies than 500 Hz can not or not accurately be cancelled because higher frequencies are to fast and are hard to predict. The TSS is able to cancel vibrations signals up to 500 Hz. The output signal of the TSS has therefore a bandwidth of 0-500 Hz. The signal system is unable to drive the piezo actuators on its own. It can not produce the output voltage and current which is needed to drive the piezo-patches.

For a good control of the piezo actuators a piezo drive system is needed. This system forms the third part of the ANC system. The piezo driver produces a proper output signal based on the output signal of the TSS. The piezo drive system is designed to drive the piezo actuators in the right way. The system can deliver the wanted output voltage and current. Further more the piezo driver system is designed to take the electric behaviour of the piezo-patches into account.

The output signal of the piezo driver system drives the actuator piezo-patches. The actuators are, like the sensors, attached to the plate. These actuators will expand or contract depending on the applied signal. The movement of the patches causes vibrations of the plate. With the correct anti-vibration signal the vibration in the plate can be cancelled.

Fig. 1.4 The Piezo-panel.

The piezoelectric effect will be treated in the next chapter. Each piezo-panel (fig. 1.4) consists of a plate with one or more piezo-patch(es) on top of it. The plate can be made of different materials, aluminium for example. The material of the plate determines the flexibility and stiffness of the panel. This is important to know because the mechanical properties of the

panel depend on these material constants. The patch dimensions are also of importance in this subject. The panels which TNO used for testing are representative for the future panels. The test panels have an area of approximately 0.5 m^2 and a thickness of 4 mm, indicated by *H* in figure (1.4). The plate is made of aluminium with a honey comb structure. The piezo-patch has a width and length between 20-70 mm and thickness of 0.1 mm.

1.3 Requirements Active Noise Cancellation system

The main goal of the ANC system is to cancel the background noise in the airplane. For this reason several demands are made concerning the sound quality. Besides the sound criteria, certain demands are made for the mechanical properties and performance of the system. The demands for these three criteria areas are discussed in the following part.

The piezo driver uses the output signal of the TSS as its input signal. So for the input signal of the piezo driver system a signal with a bandwidth of 20-500 Hz can be expected. The human ear senses sound with frequencies of 20-20 kHz, so the bandwidth starts at 20 Hz. The input signal is considered noise free in this project.

The total ANC system should form a standard device containing all the necessary elements. The intention is to make a complete system which only has to be connected to a power supply when installed. This means that the sensors, actuators and all the systems (TSS and piezo driver) have to be attached to the panel. The amount of components used for the systems should therefore be as small as possible. So in this case "*less is better*".
One of the mechanical demands of the ANC system is that the total thickness of the panel together with the signal system and piezo driver system is not thicker than 10 mm. This required thickness means that there is only 6 mm left for both of the TSS and piezo driver.

The requirement of both the complete system and thickness leave little space for alternatives. A best solution for the design of the piezo driver system is to integrate the system on chip. An IC is very flat, can easily be attached to the panel and is only one component. Another advantage is that the TNO signal system can be integrated on the same chip or an IC-package with dual IC configuration can be used. This saves space, money and reduces the total amount of components.
For the IC design silicon-on-insulator (SOI)-based technology called A-BCD can be used. This technology allows creating low voltage and high voltage circuits on the same wafer without latch-up phenomena. This way a 60 Volt output stage could be realized on the same wafer as the 12 volt internal circuitry.

The size and type of the piezo-patches which will be used on the panel is not determined yet. Because of this, the capacitance of the different piezo elements can, according to TNO, vary between minimum 50 nF and maximum 500 nF. The piezo drive system should work correctly for all of these capacitance values. The output voltage needed to fully drive the piezo elements is approximately 120 volts. The current needed to drive the piezo element will depend on the capacitance value of the piezo. The drive current of a capacitor can be found with formula (1.1).

$$I = C_{piezo} \cdot \frac{dU}{dt} \tag{1.1}$$

The maximum current will depend on the output voltage U. The output voltage will be assumed as a sinus with 60 volt amplitude and with a frequency of 500 Hz. The maximum current which can be expected is given in formula (1.2).

$$
\begin{aligned}
I_{MAX} &= 2\pi \cdot f_{sig} \cdot C_{piezo} \cdot \hat{U} \\
&= 2\pi \cdot 500\,Hz \cdot 500\,nF \cdot 60V \\
&= 94\,mA
\end{aligned}
\tag{1.2}
$$

For the maximum piezo capacitance of 500 nF and the maximum signal frequency of 500 Hz a current of 94 mA can be expected.

Another demand is that the piezo driver takes the behaviour of the piezo into account and compensates for the unwanted behaviour of the piezo patch. The electric behaviour contains hysteresis, between input voltage and displacement, and resonance frequencies. The piezo drive system should of course be stable for all conditions. The dissipation of the system should be kept as low as possible. The high voltages could result in high dissipation which is unwanted.

The last set of requirements contains the quality demands of the output signal. As stated before the ANC acts like an audio system. The human ear is sensitive for distortion of the sound signal. Therefore a maximum Total Harmonic Distortion of 3% is wanted. Furthermore the output signal of the piezo driver should have a maximum phase shift of 5˚. Phase differences between the noise and the anti-noise signal result in an incomplete cancelling of the noise.

1.4 Tasks within the assignment

The main goal of this project is to come up with a working design for the piezo driver system. The system has to be able to drive the piezo-patch and compensate for the patch's unwanted behaviour. Of course the system design should satisfy all the given requirements and demands given in the previous section.

The assignment is divided into three parts. The first part of the assignment is to research the piezo-panel. The research is used to form a model which can be used to predict the electrical behaviour of the panel and can be used for circuit simulations. Within this project much attention is paid to the behaviour of the piezo-panel which the piezo driver system has to drive. The theory of piezoelectric material will be treated to get a good understanding of this material and its electric behaviour. A piezo element has mechanical and electrical properties which are coupled. Therefore knowledge about both properties and there coupling is needed. The piezo-panel will be driven with an electric signal. This makes the knowledge about the electric behaviour and the influence of the mechanical properties on the electric behaviour of importance.

The prerequisite constraints and research information from the first part of the assignment are used for the second stage of the project. In this part of the project different system configurations are investigated to find a fitting solution to drive the piezo-panels. The end result will give a functional design that satisfies all specifications and solves the problems found along the way. A "proof of concept" will be made by means of simulations.

Third part of the assignment is the circuit realisation of the functional system. The chosen functional system has to be designed so that the system can be integrated on chip.

The system on chip will use some standard functional blocks such as the power supply, in- and output protection circuits and other protection circuitry (e.g. temperature, current). These blocks will not be designed for the IC design but assumed to be standard available. The system is realized in silicon-on-insulator (SOI)-based technology called A-BCD. The last section of this part contains the verification of the design. This is done with simulations of the circuit design. These tests will show if the system satisfies with all requirements and demands.

1.5 Summary assignment and requirements

The assignment of this Master project can be split into three parts. These parts are:

- Research of the piezo-panel and modelling the electric behaviour of this panel. The model has to predict the electric behaviour of the piezo-panel and needs to be useable for circuit simulation.

- Research of different circuit configurations and problems which can be expected within a piezo drive system. This research is used to design a piezo drive system which is able to drive the piezo-panel with the given requirements and demands.

- The circuit of the piezo drive system has to be designed so that the system can be integrated on chip. Process technology is A-BCD. The integrated circuit design has to be simulated to check if the system satisfies all requirements and demands.

The requirements and demands for the piezo driver system are:

System electric requirements	System physical demands
• Output amplitude 60 Volt • Gain of 60 • Bandwidth 20-500 Hz • Max. phase shift 5° • Max. THD 3% • Stable for given piezo-patch range • Low dissipation • Adapted to behaviour piezo-panel	• Max. thickness 10 mm • Piezo driver system on piezo-panel • Number of components as small as possible

Table 1.1 system requirements

For the ANC system the following system specifications are known:

TSS output signal	Piezo-patch	Piezo-panel
• Amplitude of 1 Volt • Bandwidth 20-500 Hz • Considered noise free	• Capacitance 50-500 nF • Width and length 20-70 mm • Thickness 0.1 mm	• Area 0.5 m^2 • Thickness 4 mm

Table 1.2 ANC system specs.

2. Piezo-panel

To get a better understanding of the piezo-panel, the panel and the attached piezo element are studied into detail. This chapter covers the mechanical and electrical behaviour of piezo material. With the acquired theory about piezo material and laminated plate theory, two models are formed. The first model is a mathematical model which can predict the electric resonance frequencies of the piezo-panel based on the material constants of the plate and piezo-patch. The other model is an electric equivalent circuit model of the piezo-panel which can be used in circuit simulations.

The first part is a short introduction of the piezo material. The next section will contain the formulation of the mathematical model and the usefulness of this model. After the discussion of the mathematical model the following section covers the electric equivalent circuit model. The two models are compared with the measurement of the impedance characteristics of the piezo-panel, which TNO made. This information will be used to verify the correctness of the found models. The facts of the piezo characteristics and the main findings are summarized and can be found at the end of this chapter.

Because of the interaction between the electric and mechanical domain some mechanical knowledge is needed. A short explanation of the most important basic mechanical terms can be found in appendix I.

2.1 Piezo material

The piezoelectric effect was discovered by Jacques and Pierre Curie in 1880. They found that if certain crystals were subjected to mechanical stress, they became electrically polarized and the degree of polarization was proportional to the applied stress. The Curies also discovered that the same materials deformed when they were exposed to an electric field. This has become known as the inverse piezoelectric effect. The effect is practically linear, i.e. the polarization varies directly with the applied stress, and is direction-dependent, so that compressive and tensile stresses will generate electric fields and hence voltages of opposite polarity. The phenomenon is reciprocal, so that if the crystal is exposed to an electric field, it will experience an elastic strain causing its length to increase or decrease according to the field polarity.

The reason why piezoelectric materials behave this way can be found in the lattice structure of these materials. In a piezoelectric crystal, the positive and negative electrical charges are separated, but symmetrically distributed, so that the crystal overall is electrically neutral, see figure (2.1). Each of these sites forms an electric dipole and dipoles near each other tend to be aligned in regions called Weiss domains. When a mechanical stress is applied, this symmetry is disturbed, and the charge asymmetry generates a voltage across the mate-
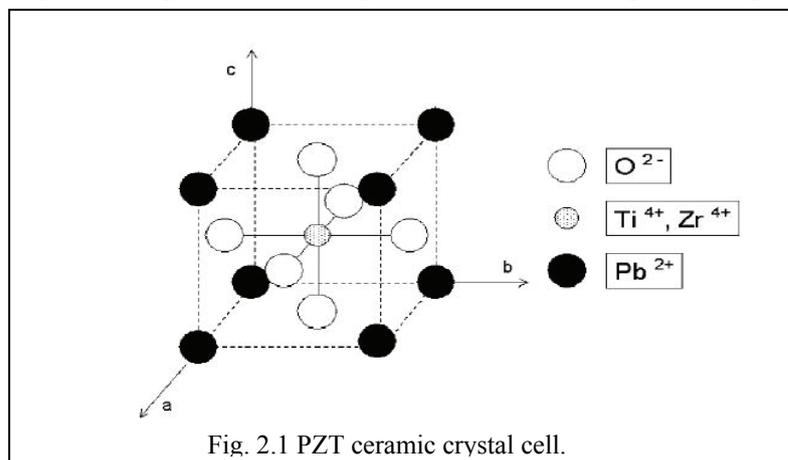

Fig. 2.1 PZT ceramic crystal cell.

rial. For example, a 1 cm cube of quartz with 2 kN of correctly applied force upon it, can produce a voltage of 12,500 V.

In terms of formula we can write $\vec{D} \approx d \cdot \vec{T}$ and $\vec{S} \approx d \cdot \vec{E}$. Where the symbols stand for:

$\vec{D}$: Electric displacement field $[N/Vm] \equiv [C/m^2]$
$\vec{T}$: Applied stress $[N/m^2] \equiv [Pa]$
$\vec{S}$: Resulting strain $[m/m]$
$\vec{E}$: Applied electric field $[V/m]$
d : Piezoelectric charge constant $[m/V]$

Besides crystals like quartz an important group of piezoelectric materials is the piezoelectric ceramics, of which PZT is an example. For further reading about the piezoelectric effect see [1], [2], [3] and [4].

The example shows that piezoelectric material can produce high voltages when mechanical stress is applied. For the inverse piezoelectric effect the opposite situation can be considered. To produce a mechanical stress a high voltage is needed. In case of the piezo-panel, the piezo-patch extends or applies stress to the plate when a voltage is applied. For a full extend of the piezo-patch a high voltage is needed. The piezo-patch which TNO tested needs a drive voltage of 120 Volts.
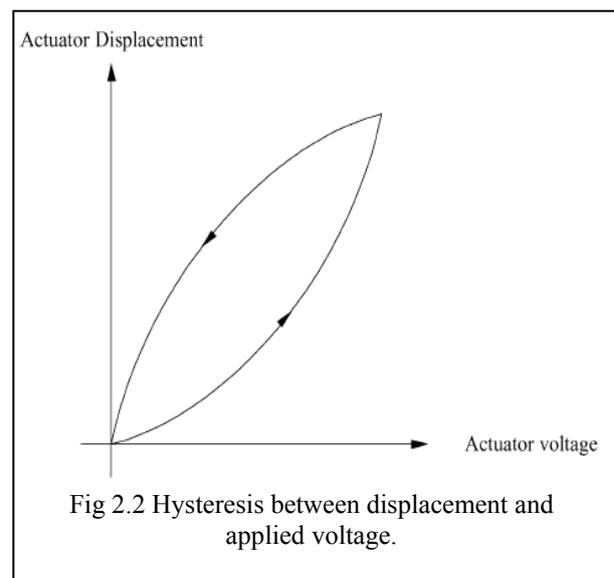
In the next part of the chapter the electrical impedance will be treated. Here it will be shown that piezo material acts like a capacitor but tends to behave more and more like a resistor for higher frequencies. For certain frequencies the piezo will even show resonance behaviour.

Beside the need of high electric fields, these high electric fields also cause nonlinearities. Because piezo ceramic materials are ferroelectric, they are fundamentally nonlinear in their response to an applied electric field, exhibiting a hysteresis effect between the displacement and the electric field [4], [5], [6]. The hysteresis curve can be seen in the graph of figure (2.2). This effect becomes more noticeable with the electric field strength [5].

On a macroscopic level hysteresis is caused by internal energy losses (or power dissipation) in piezoelectric materials when expanding or contracting.

On a microscopic level, the hysteresis can be explained by the structure of piezoelectric material. In a neutral state the Weiss domains are aligned in a certain pattern. When a high electric field is applied some of these Weiss domains are rearranged. Now when the electric field strength decreases, the domains have to get back to their original pattern. A hysteresis and nonlinear relation between the displacement and the applied electric field is the result.

The hysteresis occurs under both static and dynamic conditions, and can affect the actuator displacement by as much as 15%–20% at midloop [6]. The hysteresis may reduce the sys-

Fig 2.2 Hysteresis between displacement and applied voltage.

tem gain or bandwidth, or cause limit-cycle behaviour in a closed-loop position control system. Hysteresis forms a problem which has to be taken into account for the design. The hysteresis phenomenon is well documented and several methods exist to compensate for it, for example feed forward correction, feedback and charge control. These compensation techniques will be discussed in chapter three.

As mentioned piezo elements can resonate at certain frequencies. The resonance of piezoelectric material is related to the behaviour of elastic material. Any body of mass has certain characteristic frequencies at which it will resonate. When excited at this resonant frequency, the body will vibrate with much greater amplitude than those at other frequencies. Piezoelectric elements are no exception. Due to coupling with the electric properties of a piezo, mechanic resonance will also be manifest at the electric interface of the piezo **[1]**, **[4], [12]**.

2.2 Mathematical model piezo electrical impedance

A model is formed to be able to predict the behaviour of the impedance of the piezo element. As mentioned in the previous section, hysteresis and resonances can be expected for the piezoelectric behaviour. The hysteresis and resonance effects can form a problem for the functionality of the piezo drive system. A proper model of the piezo-panel is needed to be able to take these effects into account. Due to the electromechanical coupling nature of piezoelectric materials, the mechanical boundary conditions for the piezoelectric elements will greatly affect the electrical impedance and the circuit modelling.
The mathematical model uses the material constants to predict the behaviour of the piezo element. This gives the advantage that for other panel configurations the behaviour can be predicted. For example when a different material or thickness of the plate or piezo-patch is used, the behaviour can still be simulated with the model.
The formulation of the mathematical model of the electrical impedance of the piezo-panel consists of two parts. The first part takes a look at the behaviour of piezoelectric material and gives a formula for the electric impedance of a piezo-patch. The second part shows why and how the material constants of the piezo-patch should be altered in case the patch is part of a laminated plate, such as the piezo-panel. These two parts together will give the formula for the electrical impedance of the piezo-panel.

2.2.1 Piezoelectricity

The piezoelectric properties allow piezo transducers to be used as both actuators and sensors. When a strain is applied to a piezoelectric material a resulting electric charge is produced, and conversely an applied electric field results in a strain. There are two fundamental relations describing the piezoelectric phenomena's **[4]**, formula (2.1) and (2.2). These are:

$$\vec{D} = \varepsilon^T \cdot \vec{E} + d \cdot \vec{T} \tag{2.1}$$
$$\vec{S} = d \cdot \vec{E} + s^E \cdot \vec{T} \tag{2.2}$$

The relations are sometime also expressed as:

$$\vec{D} = e \cdot \vec{S} + \varepsilon^S \cdot \vec{E} \tag{2.3}$$
$$\vec{T} = c \cdot \vec{S} - e \cdot \vec{E} \tag{2.4}$$

Where, $[s^E] = [c]^{-1}$ (2.5)

$[d] = [e] \cdot [c]^{-1}$ (2.6)

Where the symbols stand for:

d : Piezoelectric charge constant $[m/V]$

ε^T : Dielectric constant of the medium under constant strain $[C^2/N \cdot m^2]$

ε^S : Stress transformed dielectric constant $[C^2/N \cdot m^2]$

s^E : Elastic compliance of the medium under constant electric field $[m^2/N]$

e : Piezoelectric strain/charge constant $[N/m \cdot V]$

c : Elastic stiffness constant $[N/m^2]$

$\bar{D}$: Electric displacement field $[C/m^2] \equiv [N/m \cdot V]$

$\bar{E}$: Electric field $[V/m]$

$\bar{S}$: Strain of the material $[m/m]$

$\bar{T}$: Stress working at the material $[N/m^2]$

In these equations D represents the electrical displacement, S the strain, T the stress, E the applied electric field and the constants d, ε and s represent material properties. The first equation (2.1) describes the direct and the second (2.2) the converse piezoelectric effect.
These relations form the starting point for the derivation of the impedance model [1], [4].
Formula (2.3) and (2.4) are added because these equations give the relation for the stress and displacement. Furthermore these equations show the relation with the elastic stiffness constant. In the following model derivation these will also be used.

Since piezoelectric ceramics are anisotropic, their physical constants d, ε, s, e and c are tensor quantities and relate to both the directions of the applied stress, electric field etc. and the directions perpendicular to these.
If the material is isotropic (no preferred direction), then the elasticity tensor s and the elastic stiffness tensor c can be expressed into two independent elements. These are the Young's modulus Y and the Poisson ratio v, which are both material constants. For thin plates the xy-plane is assumed to be isotropic. For s and c the following matrixes can be given [1], [10]:

$$s^E = \frac{1}{Y} \cdot \begin{bmatrix} 1 & -v & 0 \\ -v & 1 & 0 \\ 0 & 0 & 2(1+v) \end{bmatrix} \qquad c = Y \cdot \begin{bmatrix} \dfrac{1}{1-v^2} & \dfrac{v}{1-v^2} & 0 \\ \dfrac{v}{1-v^2} & \dfrac{1}{1-v^2} & 0 \\ 0 & 0 & \dfrac{1}{2(1+v)} \end{bmatrix} \qquad (2.7)$$

The dynamics of piezoelectric material, in particular its resonance frequencies, depend among other things on material constants of that particular device. When excited at this resonant frequency, the electric impedance of the piezoelectric patch will become close to zero. When describing the dynamic behaviour of piezoelectric material, compliance and inertia of the bulk material play a role.

Gereads **[1]** describes how to derive an expression for the electric impedance of the piezo. The electric impedance for a thin plate is given by formula (2.8):

$$Z_{elec} = \frac{h}{j\omega A \varepsilon^S} \cdot \left(\frac{b \cdot \cos(b) - k^2 \cdot \sin(b)}{b \cdot \cos(b)} \right) \qquad (2.8)$$

Where,

$$b = k \cdot h \qquad\qquad\qquad\qquad\qquad\qquad (2.9)$$

$$k = \frac{\omega}{v^D} \qquad\qquad \text{(Wave vector)} \qquad\qquad (2.10)$$

$$v^D = \frac{1}{\sqrt{s^D \cdot \rho}} \qquad \text{(Elastic wave speed)} \qquad\qquad (2.11)$$

$$s^D = s^E \cdot \left(1 - k^2\right) \qquad \text{(Elastic transformed dielectric constant)} \qquad (2.12)$$

$$\varepsilon^S = \varepsilon^T \cdot \left(1 - k^2\right) \qquad \text{(Stress transformed dielectric constant)} \qquad (2.13)$$

$$k^2 = \frac{d^2}{s^E \cdot \varepsilon^T} \qquad \text{(Coupling factor)} \qquad\qquad (2.14)$$

Where the symbols stand for:

h : Thickness of the piezo patch.
A : Area of the piezo patch.
ρ : Mass density of the material.
s^D : Piezoelectric strain/charge constant.
s^E : Elastic compliance of the medium under constant electric field.
ε^S : Stress transformed dielectric constant.
ε^E : Dielectric constant.
d : Piezoelectric charge constant.

The impedance formula (2.8) can be divided into two parts. The first part of the equation models the capacitance for (quasi) static behaviour, shown apart in equation (2.15). The electric impedance is the impedance of a standard capacitor. The value of the capacitance of the piezo depends on the thickness h of the patch, the area A of the patch and the dielectric constant ε. This relation for the capacitance is the same as for standard capacitors.

$$Z_{elec} = \frac{h}{j\omega A \varepsilon^S} \qquad\qquad\qquad\qquad (2.15)$$

The second part of electric impedance equation (2.8) models the resonance of the piezo. In the second part the parameter b (2.9) inserts the frequency dependents of the formula. As can be seen depends b on the wave vector k (2.10). The wave vector is frequency depended. The dynamic behaviour of the piezoelectric element is for low frequencies of no concern. This is not

the case for higher frequencies, especially for the frequencies close to the resonance frequencies. This will be shown later with the simulations.

Resonance of the piezoelectric material is related to the behaviour of elastic material [7], [8]. Due to coupling with the electric properties of a piezo, mechanic resonance will also be manifest at the electric interface of the piezo. Resonance of a piezoelectric element can be explained as follows. When a voltage is applied to the piezo, an electric field will be present in the piezoelectric element. This electric field will deform the material which causes stress in the material. When the applied voltage is removed the stress in the piezoelectric element will cause the material to vibrate. This is possible because the mass and elasticity of the material will act like al mass-spring system. Resonance occurs when the frequency of the applied voltage is the same as the frequency of the vibration of the material.

With the deduced electric impedance the resonance frequency can be found. The electric impedance has to be equal to zero for electric resonance.

Resonance: $\quad Z_{elec} = 0$ occurs when $b \cdot \cos(b) = k^2 \cdot \sin(b)$ (2.16)

The variable b, determining the resonance frequencies, depends on the boundary conditions applied. Those boundaries depend on how the plate is fixed to the world. When for instance one side of the piezoelectric material is mounted to the fixed world, the internal displacement at this side will always be zero. This boundary condition has been used for the formula deduced in text above.

The formula for the electric impedance (2.8) can be used to find the resonance frequencies but it fails to predict the height of the resonance peak. This depends on the stiffness and absorption of the panel. The absorption is not taken into account in the mathematical model. The main goal is to determine the resonance frequencies and this is possible. Fortunately simulations show that the resonance peaks are quite low. This can be seen in the measurement of the piezo-panel in the last section of this chapter.

The electric impedance formula of Gereads [1] gives a relation for the capacitance and resonance frequencies of the piezoelectric patch. However hysteresis and charge leakage of the piezo element are not accounted for. According to Guan and Liao [12] these can both be modelled as loss of energy. Guan and Liao model the losses as resistors in an equivalent circuit. The energy losses have to be implemented into the impedance model. According to the equivalent circuit which was used, the resistor modelling the hysteresis is serial to the capacitor and the resistor for charge leakage is parallel to this.

$$ Z_{elec} = \frac{\left(\dfrac{h}{j\omega A \varepsilon} + Rs \right) \cdot Rp}{\left(\dfrac{h}{j\omega A \varepsilon} + Rs \right) + Rp} \cdot \left(\frac{b \cdot \cos(b) - k^2 \cdot \sin(b)}{b \cdot \cos(b)} \right) $$ (2.17)

In equation (2.17) Rs represents the hysteresis losses and Rp the charge leakages. The addition of these losses makes the impedance model more accurate, especially for the higher frequencies. This will be shown in the simulation of the impedance model at the end of this chapter. The drawback is that the two energy loss components in the formula can not be determined with the material constants. These have to be measured for their exact value but in practise

these values will not vary very much. The overall piezo impedance characteristics show a similar frequency response.

2.2.2 Vibration of Laminated plates

The piezo-panels which are used for the ANC consist of a host plate on which a piezo-patch is bonded. The dynamics of the piezoelectric material depend as said before on the material constants (stiffness, mass density, etc.) of that particular device. The piezo-patch is now bonded to a host plate and form a laminated plate. Because of this the dynamics of the plate are altered. Vibration and resonance of the laminated plate are different in comparison with the piezoelectric patch **[7]**, **[10]**.

The resonance of a thin piezo plate depends on the Young's modulus (Y), the Poisson ratio (v) and mass-density (ρ). The new material constants for the laminated plate have to be found to be able to calculate the resonance frequency of the piezoelectric patch bonded to the host plate. The new material constants can be found by using "Classical Laminated Plate Theory" (CLPT) **[10]**, **[11]**. This theory describes how the different constants can be derived for a laminated plate. For plates which do not posses piezoelectric properties the only constants which are of interest are the elastic constant (Young's modulus Y) and the mass-density (ρ). For piezoelectric plates the dielectric constant (ε) and the piezoelectric charge constant (d) are also of importance. The piezoelectric charge constant d does not alter for the laminated plate. The transformed dielectric constant depends on the coupling factor of the piezoelectric element, which on his turn depends on the elastic stiffness constant. So the transformed dielectric constant does alter.

For the mass-density the CLPT uses the following formula **[10]**:

$$\rho_{eq} = \frac{1}{h_{tot}} \cdot \Sigma h_k \cdot \rho_k \tag{2.18}$$

The equivalent mass-density depends on the sum of the mass-density of the k layers proportional to the height of each layer k.
The elastic constant can be calculated in a similar way. But this would give a constant which is calculated by taking the total stress of the laminated plate. The total stress is in this case not of importance but the stress inside the piezoelectric element is. Figure (2.3) shows this.
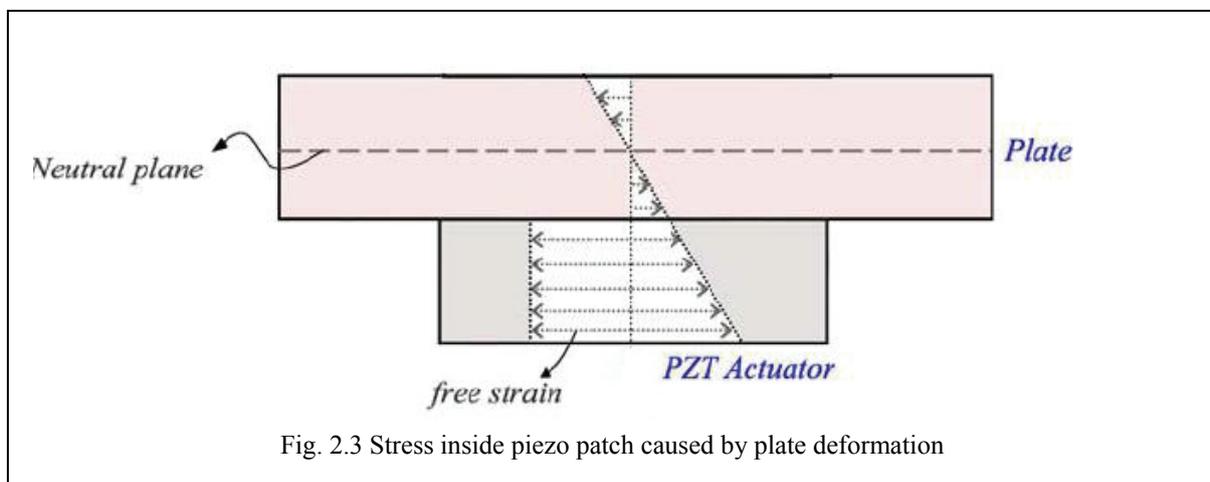

Fig. 2.3 Stress inside piezo patch caused by plate deformation

The stress inside the piezo due to vibration of the panel depends on the height and elastic constant of the piezo-patch and host plate. Yong Keat Lee **[9]** has found a solution to calculate the stress inside the piezo. He derived the following formula.

$$T_x = k \cdot T_{px} \quad \Rightarrow \quad T_{px} = \tfrac{1}{k} \cdot T_x \qquad (2.19)$$

$$T_y = k \cdot T_{py} \quad \Rightarrow \quad T_{py} = \tfrac{1}{k} \cdot T_y \qquad (2.20)$$

With k,

$$k = \frac{12 \cdot Y_p \cdot h_p \cdot (h_p + h_{host})}{24 \cdot D \cdot (1 - p_p)^2 + Y_p \cdot \left[(h_{host} + 2 \cdot h_p)^3 - h_{host}^3 \right]} \qquad (2.21)$$

$$D = \frac{Y_{host} \cdot h_{host}^3}{12 \cdot (1 - p_{host}^2)} \qquad (2.22)$$

The subscripts x and y represent the stress (T) in the x and y-direction. The subscript p indicates the piezo-patch and subscript *host* stands for the host plate. The constant p represents de Poisson ratio of the material.

The stress inside the piezoelectric element is a factor k of the total stress in the laminated plate. So when the laminated plate is stressed by an external force or by the piezo-patch itself, the piezoelectric element only experiences a factor k of the total stress.

This factor can be translated to the elastic stiffness constant of the piezoelectric element. The equivalent elastic constant for the piezo-patch bonded on the host plate becomes a factor k of the normal elastic constant.

So summarizing, for the equivalent constants of the piezo-patch bonded on the host plate, the following formulas are found:

$$\rho_{eq} = \frac{1}{h_{tot}} \cdot \Sigma h_k \cdot \rho_k \qquad (2.23)$$

$$c_{eq} = k \cdot c_p \qquad (2.24)$$

With this transformed constants for the laminated piezoelectric element the electric impedance can be found. With the equivalent constants the electric impedance (2.17) stays in the same form only some of its material constants have to be adjusted.

Now with, $\quad s_{eq} = \tfrac{1}{k} \cdot s^E \qquad (2.25)$

$$v_3^D = \frac{1}{\sqrt{s^D \cdot \rho_{eq}}} \qquad (2.26)$$

The elastic compliance has to be adjusted with a factor k, this gives the formula of (2.25). This can be understood with the knowledge that the equivalent stiffness (2.24) relates to the elastic compliance given by formula (2.7). The elastic wave speed (2.26) depends on the equivalent mass-density and indirect on the equivalent elastic compliance. Further more has the elastic

compliance influences on the elastic transformed dielectric constant (2.12), the stress transformed dielectric constant (2.13) and the coupling factor (2.14).

2.2.3 Summary mathematical model

The mathematical model has been derived to predict the electrical behaviour of the piezo-panel. The result is an impedance model of the plate based on the material constants of the host plate and the piezo-patch. The energy losses due to hysteresis and charge leakages can however not be calculated with the material constants. These parameters in the model have to be measured. But for practical piezo elements these parameter values do not vary much. In other words, the impedance frequency response shows a similar form in the frequency response. The piezo acts like a capacitor for lower frequencies and for higher frequencies like a resistor.
The model can be used to calculate the capacitance of the piezo element and the resonance frequencies. Further more the model simulates the energy losses due to hysteresis, charge leakage etc.

2.3 Equivalent circuit model

For a good understanding on the electrical behaviour of the piezoelectric ceramics a circuit model is needed. For the design and simulations of the piezo-based system a good equivalent circuit model is critical.

Without considering the energy dissipation, piezoelectric ceramic actuators are often simply considered as capacitances in their equivalent circuit models. The piezo element can be seen as two electrodes with a dielectric in between, which functions as a capacitor. This is the simplest model which can be used to model a piezoelectric element but is for many applications not sufficient enough.

Piezo ceramic elements have certain resonance frequencies at which the impedance of the elements becomes close to zero. The "Van-Dyke Model" is able to model these resonance frequencies **[8]**.
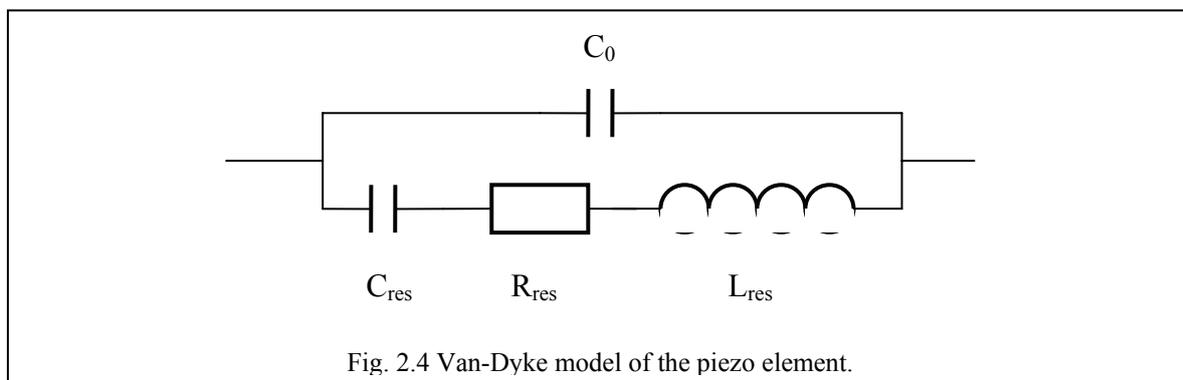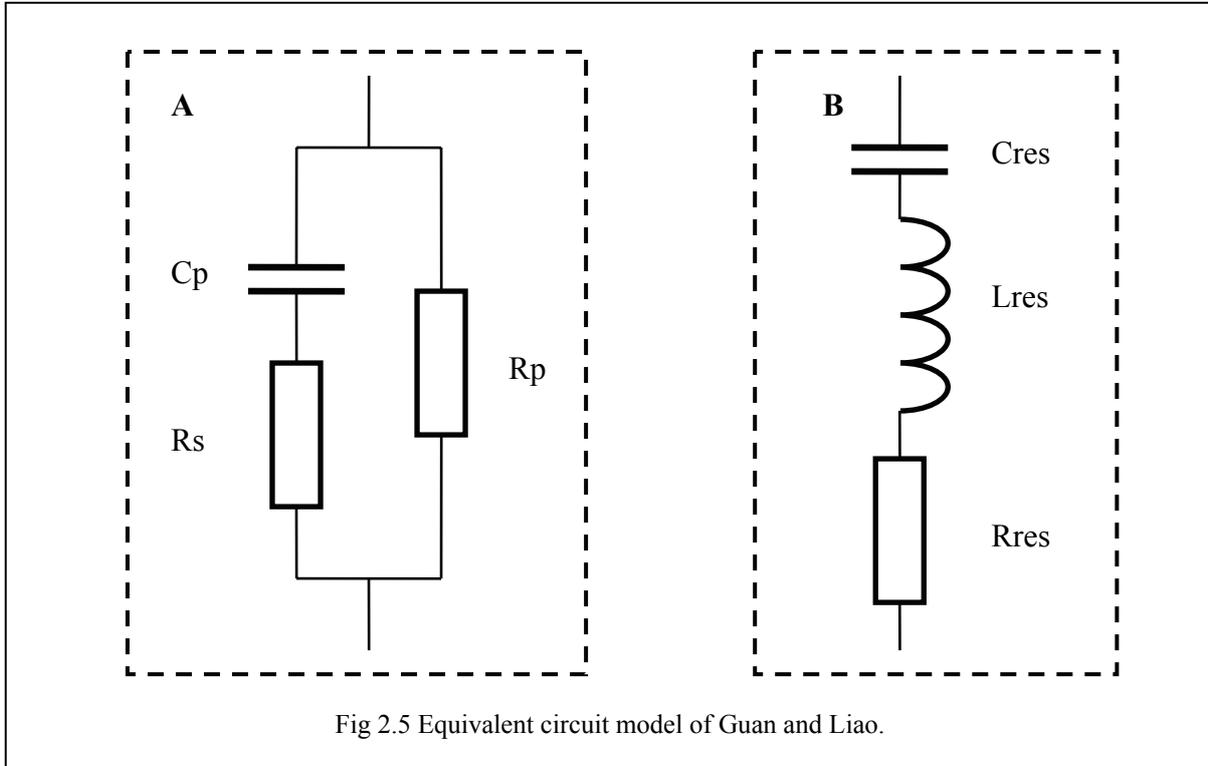

Fig. 2.4 Van-Dyke model of the piezo element.

This equivalent circuit (fig. 2.4) uses a capacitor to model the main capacitance of the piezo element and has a resonance branch in parallel to model the piezo element at resonance frequencies. An element has several resonance frequencies. Each of these frequencies is modelled with its own resonance branch.

In many applications the energy dissipation of the piezoelectric elements themselves should be considered. Therefore a more accurate circuit model for the piezoelectric ceramics actuator with the consideration of energy dissipation is desired. Guan and Liao [12] have done research in this area. They combined models to form a new model which is much more accurate, especially for the frequencies before the first resonance frequency.

Fig 2.5 Equivalent circuit model of Guan and Liao.

The model of Guan and Liao can be seen in figure (2.5). The model is divided into two parts. One part simulates the non-resonance impedance of the piezo, part A in figure (2.5). The other part (part B) is the resonance branch from the "Van-Dyke Model" which is added to the simulates the resonance frequencies of the piezo element. For each resonance frequency a resonance branch has to be used.

The adding of the resistors R_p and R_s can be explained as follows. Component R_p is responsible for the internal charge leakage, which is related to the energy dissipation. The reason for the placement of the series resistor R_s has to do with the fact that piezoelectric ceramics is a ferroelectric material. This material possesses a hysteretic and nonlinear relationship between electrical displacement D and electrical field E. The component R_s is correlated with the energy dissipation in the hysteretic D-E relationship.

The value of the components can be found by using the equations found for the mathematical model. The total capacitance of the piezo element can be found with formula (2.15). The total capacitance consists of the dominant capacitor (C_p in fig. 2.5) plus the capacitors (C_{res} in fig. 2.5) used in the resonance branches.
The two resistors (R_s and R_p) have to be measured for a precise value. The resonance branch of the equivalent circuit model is adapted to the resonance frequency. The exact frequency can be found with equation (2.16) and formula (2.30) can be used to find the ratio for the resonance components C_{res} and L_{res}.

The ratio value of the components L_{res} and C_{res} are relevant to the resonant frequency f_r by the following equation:
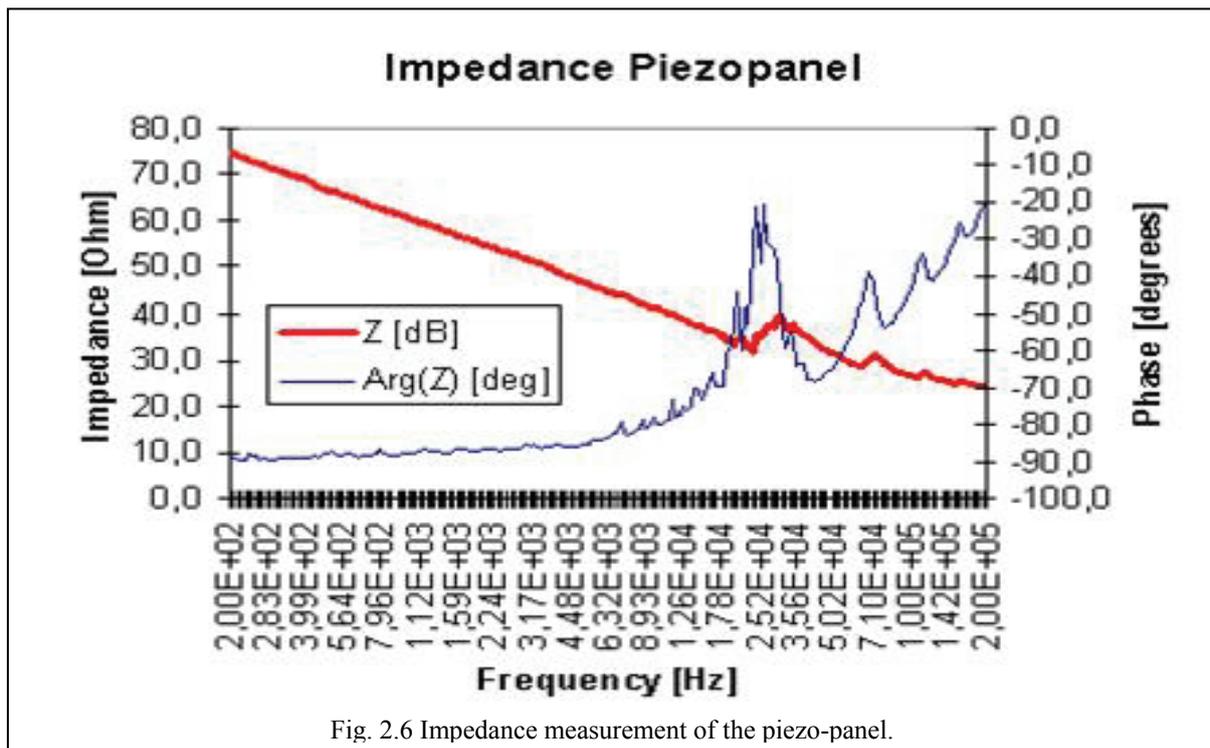
$$f_r = 1/(2\pi\sqrt{L_{res}C_{res}}) \tag{3.30}$$

The value of the C_{res} can be chosen to fit the total piezo capacitance. The value of L_{res} is than chosen to get the correct resonance frequency.
The value of R_{res} is depended on the damping of the resonance peak. The stiffness and absorption of the plate play an important role in this. The damping of the plate is great enough to ensure that no high resonance peaks will occur. The value of R_{res}, it can be adjusted so that the peak is damped in accordance with the measurement data.

2.4 Comparison of the models and measurement

The comparison of the mathematical model and the equivalent circuit model with a reference is needed to check the correctness of the two models. The measurement will first be studied to point out the most important aspects of the behaviour of the piezo-panel. The two models will be compared with these aspects.

Fig. 2.6 Impedance measurement of the piezo-panel.

A plot of the impedance measurement can be found in figure (2.6). In appendix II a magnification of the plot can be found. The horizontal axe shows the measured frequency bandwidth. The impedance scale, left vertical axe, is given in dBΩ. The impedance of the piezo is approximately 72 dBΩ at 200 Hz and for 200 kHz around the 30 dBΩ.
On the right vertical axe the phase shift is shown in degrees. The measured phase shift of the piezo element starts at -90° and stops at approximately -20°.

The first value which can be deduced from the measurement is the capacitance value of the piezo. At 200 Hz the impedance is 72 dBΩ or 3980 Ω. With the standard formula (2.31) for capacitors the capacitance of the piezo can be calculated.

$$Z_{capacitor} = \frac{1}{j\omega C}$$

(2.31)

With the values for the impedance, 3980 Ω at 200 Hz, the capacitance of the piezo is 200 nF. The capacitive behaviour of the piezo is clearly shown in the first part of the plot. Until 5 kHz the plot shows a first order slope of the impedance curve and 90° phase shift. After this frequency the phase begins to change due to the first resonance frequency at approximately 20 kHz and the influences of the energy losses.

At higher frequencies the piezo starts acting like a resistor. The slope of the impedance decreases until a constant value for the impedance is reached at approximately 28 dBΩ. Also the phase shift decreases with the frequency and tends to go to 0° phase shift for the piezo. The impedance and phase shift show that for higher frequencies (>200 kHz) the impedance of a piezo can be modelled with a resistor. So for lower frequencies the piezo acts like a capacitor while for higher frequencies the piezo can better be modelled with a resistor. The impedance of the piezo is for the higher frequencies approximately 28 dBΩ which gives a value of 25 Ω.

The last obvious aspect of the piezo impedance is the resonance of the piezo-panel. There are in total five frequencies where the panel resonates. Only the first two can clearly be seen in the impedance curve. The phase curve shows the resonant frequencies a lot better. The first four resonances are easy to see. The last frequency is around the 200 kHz and is therefore not shown completely. The five frequencies are; 20 kHz, 70 kHz, 100 kHz, 160 kHz and 200 kHz. Further study of the impedance curve shows low peaks at the resonance frequencies. The highest peak can be expected at the first resonance frequency. The peaks of the second, third etc. frequency will become lower and lower. From this observation the assumption can be made that for higher frequencies (> 200 kHz) the resonance of the piezo-panel can be neglected.

The found impedance characteristics of the piezo-panel will now be used to check correctness of the mathematical model and the equivalent circuit model. To ease the comparison the same frequency band, used in the measurement, will be used for the simulation of the two models. The impedance will for the same reason be displayed in dBΩ. As first the mathematical model will be discussed.

Material constants		PZT (piezo-patch)	Aluminium (host plate)
Length / Width	[mm]	40	700
Thickness	[mm]	0.1	4
Mass-density	[kg/m³]	7500	2700
Young Modulus	[kN/mm²]	$60.6 \cdot 10^9$	$69.9 \cdot 10^9$
Poisson ratio		0.33	0.3
Coupling factor		0.42	
Dielectric constant		1900	

Table 2.1, Material constants of the piezo-patch and host plate.

The mathematical model makes use of the material constants of the piezo element and the plate. The material constants can be found in table (2.1) For the simulation the material constants of PZT are used. This piezo material is used often for piezoelectric sensors and actua-

tors. The plate of the test panel is made of aluminium. Furthermore the sizes of the test panel have been used for this simulation.

The last two values needed are those of the loss factors R_s and R_p. The R_p models the charge leakage and is therefore quite high, in the order of mega ohms. For R_s the values of 25 Ω is taken. For R_p a similar value as used in [12] is chosen, 8 MΩ.

The formula (2.17), together with the calculated equivalent constants (equation (2.25) and (2.26)), is used to simulate the mathematical model. The simulation is done with Maple, see appendix III for the maple sheet. Figure (2.7) shows the simulation of the model, appendix IV shows an enlarged plot.

When comparing the mathematical model with the reference measurement the resemblance can easily be seen. The little differences are probably caused by the little differences between the chosen material values and the real material values. The value of the impedance at 200 Hz in the mathematical model is approximately 70 dBΩ. Using formula (2.15), the capacitance of the piezo is 223 nF. This value is very close to the capacitance value of 200 nF which was derived from the reference measurement. The overall form of the impedance curve in the mathematical model is also very similar to that of the reference model.

For low frequencies the capacitive behaviour dominates and for the higher frequencies the modelled piezo acts more like a resistor. The added resistors in the piezo model do give a realistic prediction of the piezo impedance. For higher frequencies the mathematical model is more accurate because of the resistors.

The main difference between the mathematical model and the reference measurement are the high resonance peaks. The absorption of the plate has not been modelled. This causes the high peaks. The resonance frequencies are however in both the model as in the measurement, more or less the same.
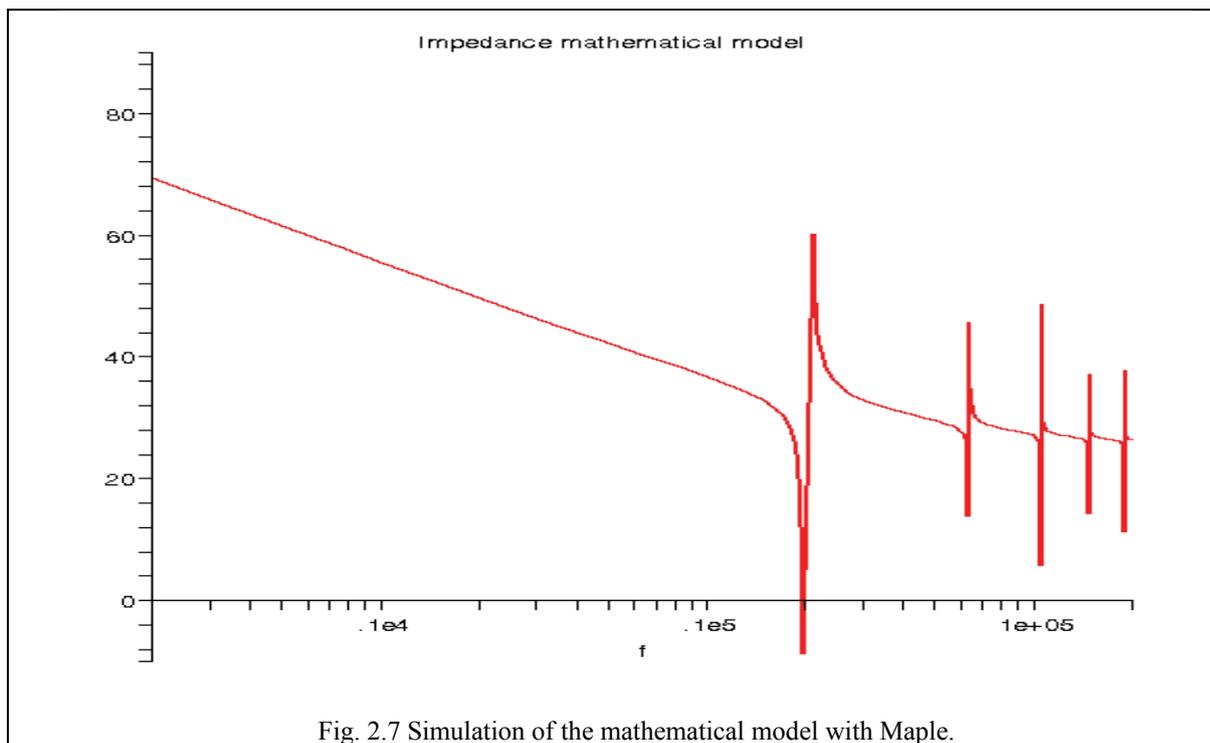

Fig. 2.7 Simulation of the mathematical model with Maple.

The peaks of the resonances are not the same in both impedance curves but that is not considered to be a problem. The form of the impedance graph, capacitance and resonance frequencies are very similar to the reference measurement. Prediction of these aspects of the impedance was the main goal of the mathematical model. The model can therefore be considered correct.

The equivalent circuit model has also to be checked. This model will be used in circuit simulations. For the design and simulation of the circuits a correct equivalent circuit model is needed. The equivalent circuit model of Guan and Liao (fig. 2.5) is used. This model will be compared to the reference measurement. The capacitance and the resonance frequencies are calculated with the help of the mathematical model. The calculations are then used to determine the value of the components.

			Res. 1	Res. 2	Res. 3
Cp	125 nF	Cres	75 nF	15 nF	8 nF
Rs	25 Ω	Lres	1 mH	375 μH	316.5 μH
Rp	8 MΩ	Rres	35 Ω	45 Ω	65 Ω

Table 2.2, Component values for the equivalent piezo circuit.

For the simulation only the first three resonances are considered. The other two have little influence on the behaviour. The resonances at 20 kHz, 70 kHz and 100 kHz are simulated. The total capacitance of Cp plus the three Cres gives a capacitance of 223 nF. The values of resistors in the resonance branches are chosen with 'trail and error' to get an impedance curve similar to the reference measurement. The equation of (2.30) is used to find the proper value for the capacitor and inductor for each resonance branch. The value of Rs is taken from the measurement.

The simulation of the equivalent circuit is done with Cadence. The result can be seen in figure (2.8) and in appendix V. On the left vertical axe the impedance of the piezo element is shown in dBΩ. The right vertical scale shows the phase characteristics of the piezoelectric element.
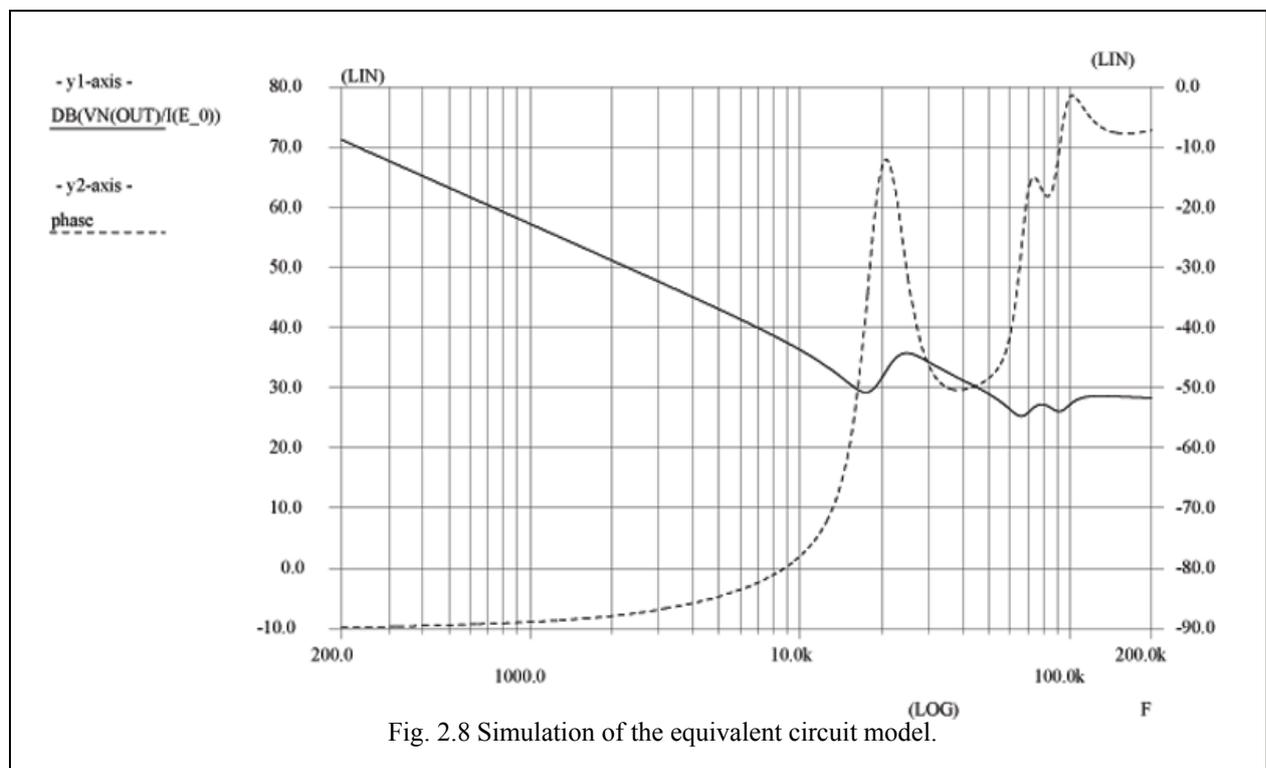

Fig. 2.8 Simulation of the equivalent circuit model.

The impedance curve of the equivalent circuit model shows a similar as the curve of the reference measurement. The biggest difference between the circuit model and the reference is mainly caused by the lack of the last two resonance frequencies and the value of the resistors in the resonance branches. The shape of the impedance curve shows a capacitive behaviour for the lower frequencies and resistance behaviour for the higher frequencies. The impedance value at 200 Hz is around 71 dBΩ. This is obvious because the same value for the capacitance was used which was calculated for the mathematical model. The capacitance used in the circuit model is therefore close to the capacitance of the measured reference piezo-panel.

With the correct values, the equivalent circuit model can be used for simulations. The impedance behaviour of the model is the same as for the reference measurement.

2.5 Summary Piezo-panel

In this chapter the piezoelectric theory is discussed. This theory has been used to get some understanding in the electric behaviour of the piezo-panel.

Two models have been formed to predict the behaviour of the piezo-panel. The first model, mathematical model, predicts the impedance behaviour based on material constants. The second model can be used for circuit simulations. This model uses calculated values from the mathematical model. Comparison with a reference measurement shows that both models show similar frequency response for the impedance and phase characteristics.

The knowledge which is acquired in this chapter will be used to design the piezo driver system.

3. Functional design

The problems of hysteresis and resonance have been discussed in chapter one and two have to be solved in the system design. Different functional designs are researched in this chapter to find the best or most fitting solution for the problems. The research results in a system which can operate within the given specifications and compensates for the problems. In chapter two the requirements and demands of the system have been discussed. Chapter one and two form the guideline for the research and the design of the functional design. This chapter discusses the functional design, the research of the design and the steps which were made along the way.

3.1 Main function

In chapter two the first major choice for the main system design was already made. The requirement to form a complete system where the piezo driver system has to be attached to the panel plus the maximum thickness of the piezo-panel leads to choice to integrate the system on chip. This choice however gives an extra criterion for the design of the system. For example the maximum capacitance which can be used will be around 10 pF. Some of the implementation problems can be solved by placing components with excessive values outside the IC. However the intention is to keep the amount of components on the panel as small as possible.

The piezo driver system is needed because the signal system of TNO can not provide the voltage and current to drive the piezo-panel. An output voltage of 60 volts is needed with a current of almost 100 mA. The high output voltage level requires the use of a process technology which can handle the high and low voltages. The silicon-on-insulator (SOI)-based technology called A-BCD is used for the IC design. In this technology transistors are available called DMOST which can withstand the required voltages. This way a 60 volt output stage can be realized.

The input voltage of the piezo driver is 1 Volt and the piezo drive system has to deliver an output voltage of 60 Volt. In other words this requires the use of an amplifier. The main function of the piezo driver will therefore be a power amplifier. Several power amplifier designs exist, each with there own advantages and disadvantages. In this assignment the class-A, class-B, class-AB and class-D amplifier are investigated. Beside the amplifier topologies a charge pump configuration is also investigated. At the end of this section all the topologies will be compared with each other and the best configuration will be chosen.
The research focuses on two aspects of the amplifier types to find the best choice for the piezo driver system. The greatest difference between the amplifiers can be seen in the power dissipation and distortion of the output signal. The human hearing is sensitive to distortion of the sound because of this the distortion should be kept as low as possible. The output signal quality requires a distortion of maximum 3% THD.
The dissipation of the amplifiers should also be kept as low as possible. There are two reasons for this. The first reason is the total dissipation by all piezo-panels can become too large.
For example; when the piezo-panel makes use of 4 piezo-patches than also 4 piezo drive systems have to be used. If 50 panels are needed in a cabin, a total of 200 piezo drivers will be active. The total dissipation for a piezo drive system which uses 10 W will then be 2000 W!
For a 1 W system the total dissipation will only be 200 W. The difference in dissipation be-

tween a 10 Watt system and a 1 Watt system is quite a lot, 1800 Watt. This gets worse when more piezo-patches and/or panels are needed. High dissipation is unwanted and just a waste of energy.

The second reason to have a low dissipation is because the system will be integrated on chip. An IC-package is limited in the amount of heat/energy which it can radiate to its environment. If the rate at which energy is dissipated in a device is less than the rate at which it is generated, the temperature of the device must rise. In electronic devices, electrical energy is converted to heat energy at a rate given by $P = V \cdot I$ Watt, and temperature rises when this heat energy is not removed at a comparable rate. Since semiconductor material is irreversible damaged when subjected to temperatures beyond a certain limit, temperature is the parameter that ultimately limits the amount of power a semiconductor device can handle. A normal value which an IC-package can dissipate is about 1 to 5 Watt.

The radiation of heat can be improved by equipping the IC-packages with heat sinks. These are attached to the package and conduct heat outwards. The piezo-panel plate itself could function as heat sink. This however works only when the plate is made of a material with a low heat resistance. Because the material for the plate is not decided on yet, this solution cannot be used. Equipping the IC-package with a heat sink is also not possible. The required maximum thickness of 10 mm for the piezo-panel prohibits the use of heat sinks.

3.1.1 Class-A amplifier

Class-A amplifiers amplify over the whole of the input cycle such that the output signal is an exact scaled-up replica of the input with no clipping [13]. Figure (3.1) shows a circuit implementation of a class-A amplifier. These amplifiers are the usual means of implementing small-signal amplifiers. They are not very efficient. This is not a problem for small signals, the waste of power is still extremely small, and can be easily tolerated. Only when output powers with appreciable levels of voltage and current are needed, the class-A becomes problematic. In case of the piezo driver system this forms a problem. In a class-A circuit, the amplifying element is biased such that the device is always conducting to some extent, and is operated over the most linear portion of its characteristic curve. Because the device is always conducting, even if there is no input at all, power is wasted. This is the reason

Fig. 3.1 Class-A amplifier circuit.

for its high dissipation. The dissipation of a class-A amplifier is given in formula (3.1). In this formula Vss is taken as $-Vdd$.
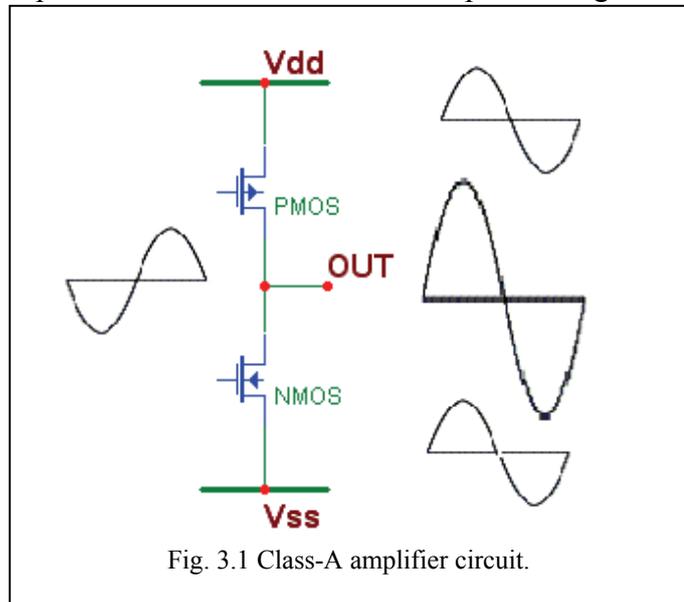
$$P_{Class-A} = 2 \cdot Vdd \cdot Ibias \qquad (3.1)$$

The dissipation equation of the class-A is derived in appendix VI. With a supply voltage (Vdd) of 60 Volt and a minimum bias current ($Ibias$) of 94 mA, see equation (1.2), the class-A amplifier dissipates 11.3 Watt. This is far too much dissipation.

3.1.2 Class-B amplifier

Class-B amplifiers only amplify half of the input wave cycle. As such they create a large amount of distortion, but their efficiency is greatly improved and is much better than class-A. Class-B has a maximum theoretical efficiency of 78.5% for a resistor as load and sinusoidal input signal [13]. This is because the amplifying element is switched off altogether half of the time, and so cannot dissipate power, see figure (3.2).

A single class-B element is rarely found in practice. A practical circuit using class-B elements is the complementary pair or "push-pull" arrangement. Here, complementary devices are used to each amplify the opposite halves of the input signal, which is then recombined at the output. This arrangement gives excellent efficiency, but can suffer from the drawback that there is a small glitch at the "joins" between the two halves of the signal. This is called crossover distortion. Distortion is unwanted for the piezo driver system. In a normal class-B operation the com-

Fig. 3.2 Class B amplifier circuit.

plementary devices each amplify a half of the voltage input signal. This is however not possible for the piezo driver system. The piezo-panel has a capacitive behaviour for the lower frequencies and since the input signal of the piezo driver has a maximum frequency of 500 Hz, the load of the system can be assumed to be a capacitor.

To increase the output voltage, charge should be added to the capacitor. The PMOS, in figure (3.2), needs to conduct the current from *Vdd* to the output. For the decrease of the output voltage, charge should be removed form the capacitor. The current can flow from the output to *Vss* when the NMOS is active. Thus for a capacitor as output load the complementary devices each need to conduct a half of the current signal. A capacitor causes a 90° phase shift between the output current and output voltage. This can be seen in figure (3.3). Because of this the voltage over the transistors is doubled when it starts conducting. This leads to an increase in the dissipation.
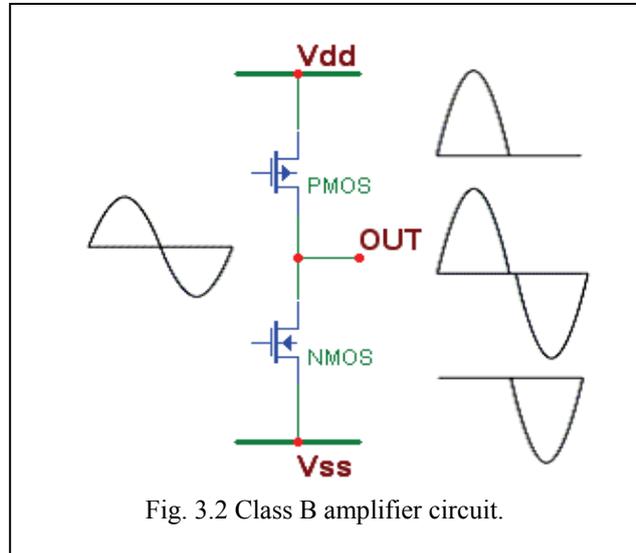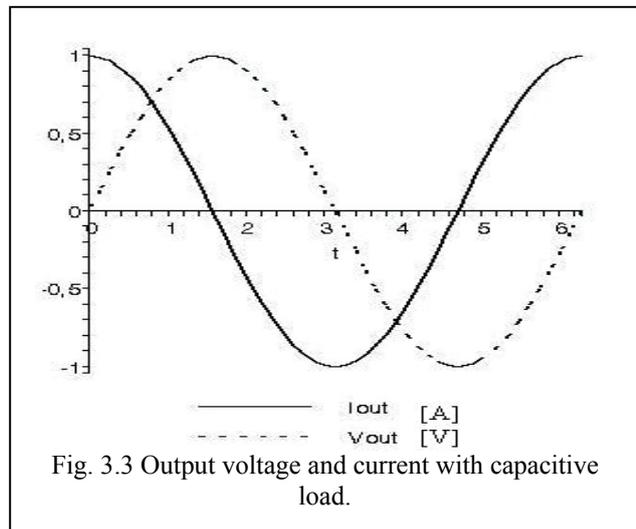

Fig. 3.3 Output voltage and current with capacitive load.

The dissipation can be calculated using formula (3.2), the derivation of the equation is made in appendix VI. In the derivation the negative supply (*Vss*) is taken as −*Vdd*.

$$P_{Class-B} = \frac{4\omega \cdot C_{LOAD} \cdot A \cdot Vdd}{\pi} \qquad (3.2)$$

35

In equation (3.2) *A* is used for the amplitude of the output signal. The maximum dissipation occurs when the output signal is also at maximum, *A = Vdd*. For the piezo driver system the dissipation with a class-B would be:

$$P_{Class-B} = \frac{4 \cdot 2\pi \cdot 500\,Hz \cdot 500\,nF \cdot 60V \cdot 60V}{\pi} = 7.2\,Watt \qquad (3.3)$$

The dissipation of a class-B would be 7.2 W. This is better than the dissipation of a class-A amplifier but at the cost of the output signal quality.

3.1.3 Class-AB amplifier

A solution to the distortion of the class-B amplifier is to bias the devices just on, rather than off altogether when they are not in use. This is called class-AB operation. Each device is operated in a non-linear region which is only linear over half the waveform, but still conducts a small amount on the other half. Such a circuit behaves as a class-A amplifier in the region where both devices are in the linear region, however the circuit cannot strictly be called class A if the signal passes outside this region, since beyond that point only one device will remain in its linear region and the transients typical of class B operation will occur. The result is that when the two halves are combined, the crossover is greatly minimized or eliminated altogether. The distortion is therefore minimal or not at present at all. However, it is important to note that while the distortion of class-AB is less than class-B, the dissipation of class-AB is greater than class-B.
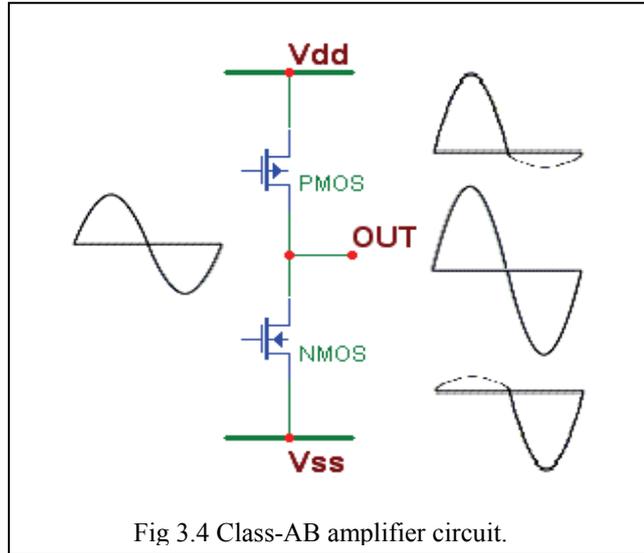

Fig 3.4 Class-AB amplifier circuit.

The dissipation of a class-AB amplifier can be calculated with formula (3.4). This is for a great part the same equation as for the class-B amplifier. The dissipation of the bias current is added. A class-AB amplifier is in most cases biased at 1% of the peak value of the current **[13]**. In chapter two the peak current is calculated, in equation (1.2), at 94 mA. A bias current of 1 mA is taken. The total dissipation of class-AB is 7.32 Watt.

$$P_{Class-AB} = \frac{4\omega \cdot C_{LOAD} \cdot A \cdot Vdd}{\pi} + 2 \cdot I_{BIAS} \cdot Vdd \qquad (3.4)$$

$$P_{Class-AB} = \frac{4 \cdot 2\pi \cdot 500\,Hz \cdot 500\,nF \cdot 60V \cdot 60V}{\pi} + 2 \cdot 1mA \cdot 60V$$
$$= 7.32\,W \qquad (3.5)$$

As said the dissipation of the class-AB is greater than class-B amplifier. The difference between the two is however not very great.

3.1.4 Class-D amplifier

A class-D amplifier is a power amplifier where all power devices are operated in on/off mode. These amplifiers use pulse width modulation, pulse density modulation. The input signal is converted to a sequence of pulses whose averaged value is directly proportional to the amplitude of the signal at that time. Figure (3.5) shows a simple representation of a class-D circuit. The frequency of the pulses is typically ten or more times the highest frequency of interest in the input signal.

The output of such an amplifier contains unwanted spectral components (i.e. the pulse frequency and its harmonics) that must be removed by a passive filter. For a proper function of the amplifier the filter with a coil is needed. Coils are however not easy to make on an IC, especially for larger inductance values, and can therefore better be placed outside an IC. The resulting filtered signal is then an amplified replica of the input.
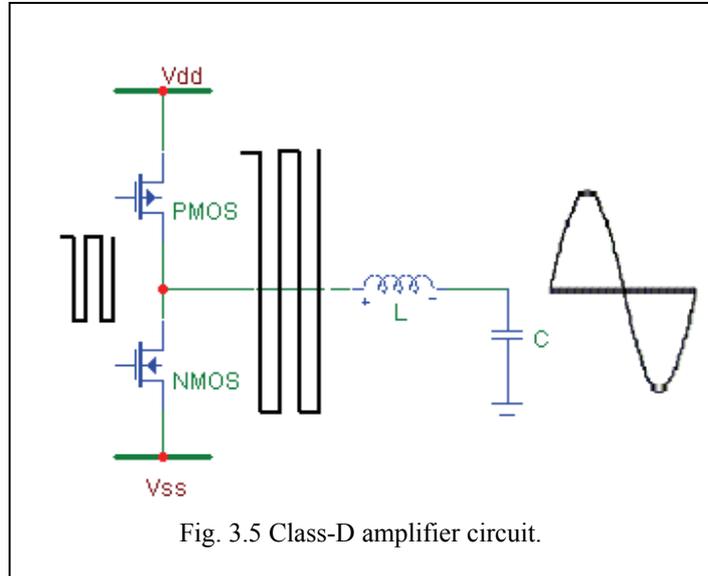

Fig. 3.5 Class-D amplifier circuit.

The main advantage of a class-D amplifier is low power dissipation. Because the output pulses have fixed amplitude, the switching elements (usually MOSFETs) are switched either on or off, rather than operated in linear mode. This means that very little power is dissipated by the transistors except during the very short interval between the on and off states. The wasted power is low because the instantaneous power dissipated in the transistor is the product of voltage and current, and one or the other is almost always close to zero. These losses are called the conduction losses. The other form of dissipation in a class-D amplifier is caused by the switching of the transistors.

The output transistor size is chosen to optimize power dissipation over a wide range of signal conditions. Ensuring that the voltage drop over the transistors stays small when conducting large current requires the on resistance of the output transistors to be small (typically 0.1 V to 0.2 V) **[14]**. But this requires large transistors with significant gate capacitance.

The gate-drive circuitry that switches the capacitance consumes power. This "switching loss" becomes excessive if the capacitance or frequency is too high, so practical upper limits exist. The choice of transistor size is therefore a trade-off between minimizing conduction losses during conduction vs. minimizing switching losses. The total dissipation of a class-D amplifier can be calculated with formula (3.6) **[15]**, **[16]**.

$$P_{Class-D} = P_{SW} + P_{GD} + P_{COND} \qquad (3.6)$$

The switching losses are P_{SW} and P_{GD}. The first term, P_{SW}, represents the transition losses when switching from on/off or off/on. During the off/on transition the drain-source voltage changes from VDS(off) to 0 Volt and the current is ramping from 0 A to the load current, while in the on/off transition interval the drain voltage is falling from 0 Volt to near VDS(off) and the load current falling to 0 A.

The transition losses can be approximated with equation (3.7) [15].

$$P_{SW} = \frac{Vdd \cdot I_{RMS} \cdot (t_1 + t_2)}{2 \cdot T} \qquad (3.7)$$

In this formula Vdd represents the supply voltage, I_{RMS} the load current, t_1 the off/on transition time, t_2 the on/off transition time and T the switching period. For small transition times the transition losses will be small.

During the switching of the output stage the drain-source capacitance of the transistors is charged and discharged which causes dissipation. However the drain-source is very small and therefore is the loss due to (dis)charging the drain-source very small. This loss is not considered in the switching losses.

The second switching loss effect is P_{GD}. This loss mechanism is the gate drive loss of the device. Turning-on or off the MOSFET involves charging or discharging the gate capacitor. When the voltage across a capacitor is changing, a certain amount of charge has to be transferred. The amount of charge required to change the gate voltage between 0 Volt and the actual gate drive voltage give the loss per switching cycle. The gate drive losses can be calculated using formula (3.8).

$$P_{GD} = C_G \cdot V_{GS}^2 \cdot f_{PWM} \qquad (3.8)$$

The gate-source voltage V_{GS} represents the drive voltage of the transistor, C_G the gate capacity and f_{PWM} the switching frequency of the drive pulses.

The conduction losses are determined by the load current and the on-resistance of the transistors. As said, large transistors have a small on-resistance. The conduction losses can be calculated with (3.9).

$$P_{COND} = (I_{RMS})^2 \cdot R_{ON} = I_{RMS} \cdot V_{DS} \qquad (3.9)$$

The R_{ON} represent the on-resistance of the transistor, the I_{RMS} the rms load current and V_{DS} the voltage drop over the transistor. For the calculation of the total dissipation of the class-D the following values are taken:

- $Vdd = 60\ V$
- $I_{RMS} = \frac{1}{\sqrt{2}} \cdot 94\ mA$
- $Vds = 0.2\ V$
- $f_{PWM} = 350\ kHz$

- $V_{GS} = 12\ V$
- $C_G = 200\ pF$
- $t_1 = t_2 = 700\ ns$
- $T = \dfrac{1}{f_{PWM}}$

A drain-source voltage (Vds) of 0.2 Volt [14] with a switching frequency (f_{PWM}) of 350 kHz [17] are typical values for a class-D amplifier. The gate-source voltage (Vgs) and gate capacitance (C_G) were found in DMOS file and simulation in cadence. For the transition times 25% is taken from the switch period. The total dissipation of the class-D can now be calculated with formula (3.6).

$$P_{Class-D} \approx 1\ W \qquad (3.10)$$

The calculation shows that the class-D amplifier has low power dissipation. The dissipation of class-D depends greatly on the size of the transistors and the switching frequency. The dissipation can therefore be larger or smaller with other values. However the taken values for the calculation are realistic and give therefore a realistic approximation of the power dissipation of the class-D amplifier.

The distortion of a class-D can be quite low as well when feedback is applied [14], [15], [17]. Audiophile-grade sound quality with THD < 0.01% is attainable in well-designed closed-loop Class D amplifiers [14].

3.1.5 Charge pump

A charge pump is an electronic circuit that uses capacitors as energy storage elements to create either a higher or lower voltage power source. Charge pump circuits are capable of high efficiencies, sometimes as high as 90-95% while being electrically simple circuits. This topology can also be used for the piezo driver system. The piezo element is than used as the load capacitor. Low dissipation can be achieved in this way.

Charge pumps use some form of switching device(s) to control the connection of voltages to the capacitor. For instance, to generate a higher voltage, the first stage involves the capacitor being connected across a voltage and charged up. In the second stage, the capacitor is disconnected from the original charging voltage and reconnected with its negative terminal to the original positive charging voltage. Because the capacitor retains the voltage across it (ignoring leakage effects) the positive terminal voltage is added to the original, effectively doubling the voltage. The charge is used to fill up the load capacitor. The capacitor used as the charge pump is typically known as the "flying capacitor". The pulsing nature of the higher voltage output is typically smoothed by the use of the load capacitor. This is the charge pumping action, which typically operates at tens of kilohertz to minimize the amount of capacitance required.
In case of the piezo driver system the "flying capacitor" has to be, preferably, integrated on chip. This means that this capacitor can have a maximum capacitance of 10 pF. The capacitance of the piezo-patch is 500 nF at maximum. The charge pump switching frequency should be fast enough to produce the desired output signal. The maximum slope of the output signal is calculated with equation (3.11).

$$Rc_{max} = 2\pi f \hat{V} = 2 \cdot \pi \cdot 500\,Hz \cdot 60V = 188.5K\,V\!/\!_s \qquad (3.11)$$

Next step is the calculation of the voltage increase or decrease of the load capacitor. This is referred as the *pump voltage* in formula (3.12).

$$Pump\,voltage = \frac{Ubron}{Cload\!/\!_{Cpump}} = \frac{60V}{500\,nF\!/\!_{5\,pF}} = 0.6\,mV \qquad (3.12)$$

The total periods per second can now be calculated with equation (3.13).

$$Pumpfreq. = \frac{Rc_{max}}{Pumpvoltage} = \frac{188.5\,K\,V\!/\!_s}{0.6\,mV} = 314\,MHz \qquad (3.13)$$

A switching frequency of 314 MHz is needed for the charge pump configuration. This is quite high and becomes a little to exotic for the application. A larger flying capacitor can be used outside the chip to reduce the switching frequency. This however increases the pump voltage leading to larger spikes in the current and a less smooth output signal

Furthermore the distortion of the output signal can be quite severe because of the pumping voltage characteristic. The spike current behaviour can also generate substantial noise. Charge pump are electrically simple circuits, the most complicated part of the system would be the timing of the switches and to be able to charge or discharge the load capacitor randomly.

3.1.6 Comparison and conclusion main function

In these last sections the class-A, B, AB and D as well as the charge pump topology have been discussed. The charge pump had promising behaviour for low power dissipation but requires a very high switching frequency for it. The switching frequency can be decreased by using a larger pump capacitor but this gives problems with the quality of the output signal and requires the use of external components.

The amplifier classes differ mostly in the dissipation and distortion of the output signal. The class-A amplifier produces a good quality of the output signal with almost no distortion. This is because the amplifier operates for the whole sine wave in its linear mode. The dissipation is because of this very high. The class-A amplifier dissipates 11.3 Watt continue, even with no input signal.

The class-B amplifier dissipates less than the class-A because only one of its transistors is conducting. For a load resistor this methodology has low power dissipation but with the use of a load capacitor the dissipation is increased. As calculated the dissipation for class-B would be 7.2 Watt. This is better than the class-A but still is too large. Another problem is the crossover distortion. This gives distortion of the output signal and is unwanted.

The class-AB amplifier solves the distortion problem by biasing the transistors with a small current. This increases the dissipation but cancels or almost completely cancels the distortion. The dissipation of the class-AB is just a bit larger than the class-B with 7.32 Watt. For this amplifier the dissipation is also too large.

The class-D is known for its high efficiency. The dissipation calculations showed that a class-D amplifier will use approximately 1 Watt. This is the lowest dissipation for all four amplifier classes. By applying feedback in the class-D amplifier the distortion can be kept low. Other design of class-D amplifiers have shown this. A disadvantage of the class-D is the necessity of a coil in the output filter. For a large inductance value the coil has to be an external component. This requires the use of an extra component next to the IC on the piezo-panel. However the use of one extra component on the plate is tolerable.

Comparing all the amplifier types and the charge pump configuration the conclusion can be made that the class-D amplifier is the best option for the piezo driver design. Distortion can be kept low and dissipation of power is low. The class-D operation will be discussed into further detail in the following sections.

3.2 Class-D amplifier functional design

Thanks to a different topology (figure 3.6), the class-D amplifier dissipates much less power than any of the other amplifier configurations. Its output stage switches between the positive and negative power supplies so as to produce a train of voltage pulses. This waveform is benign for power dissipation, because the output transistors have zero current when not switching, and have low drain-source voltage when they are conducting current, thus giving smaller dissipation, $Ids \cdot Vds$.

The class-D topology consist of four different functional blocks, see figure (3.6). These are the modulator, output stage, filter and feedback block. Beside the input and output signal another signal, the reference signal, is of importance for the functionality of the system.

The input signal is transformed into a pulse signal which carries the input signal information. This is done by the modulator which uses the reference signal in the process. The pulse train drives the output stage which switches between the power supplies resulting in a high voltage pulse signal. A pair of power transistors is often used as the output stage. The output filter extracts the input signal information out of the high voltage pulse train. This results in an output signal which is the amplified version of the input signal.
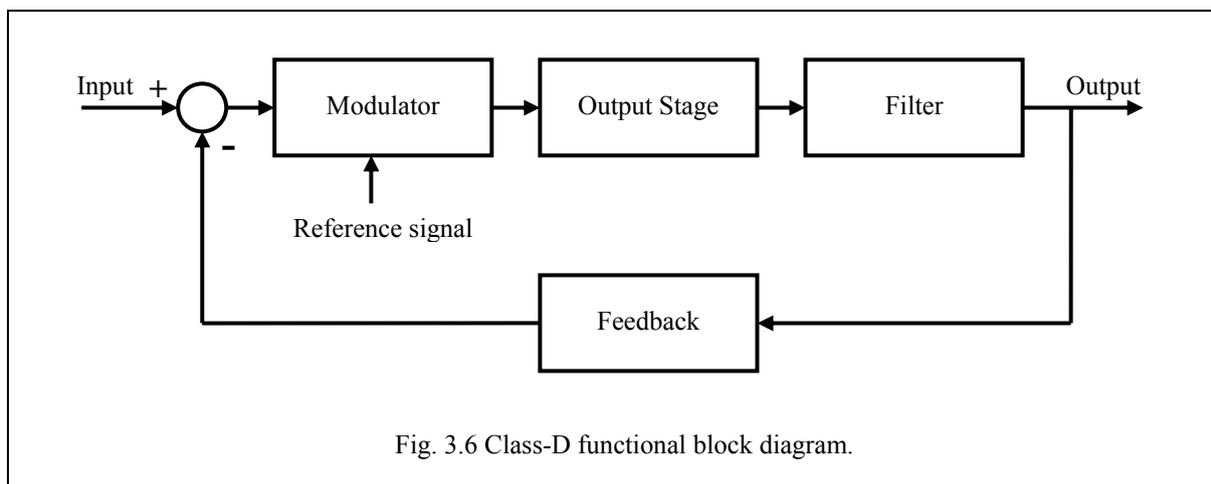
Fig. 3.6 Class-D functional block diagram.

The different functions of the blocks have been briefly discussed. The class-D amplifier has now to be adjusted to the requirements of the piezo driver system. Also compensation for the behaviour of the piezo element and use of charge control have to be implemented into the system. Therefore several of the functional blocks need further analyses and adjustments in their functionality. The output stage, pulse width modulator, filter and feedback will be further discussed in the following
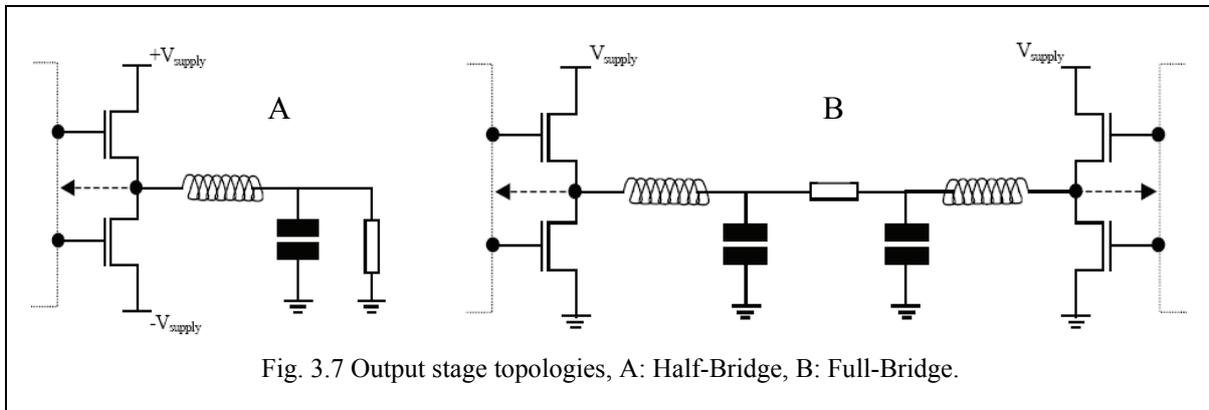
3.2.1 Output stage

The output stage switches between the supply voltages to create the high voltage pulse train. The modulator drives the output stage of the class-D amplifier, causing it to switch on and off as the pulses switch between high and low.
The output stage often requires the use of large transistors. The pulse width modulator is not designed to drive these large transistors. The output stage contains therefore the gate driver sub-function which drives the gates of the output transistors and makes sure that the two tran-

sistors are not conducting at the same time. The use of *dead time* between the switching of the output transistors ensures that the transistors are not active at the same time.

Two popular switching circuits exist for the output stage, called *half-bridge* and *full-bridge*. Figure (3.7) shows the two circuit topologies.

Fig. 3.7 Output stage topologies, A: Half-Bridge, B: Full-Bridge.

The full-bridge has two half-bridge switching circuits that supply pulses of opposite polarity to the filter, which comprises two inductors, two capacitors, and the load. Full-bridge circuits generally run from a single supply, with ground used for the negative supply terminal. For a given supply, the differential nature of the bridge means that it can deliver twice the output signal and four times the output power of half-bridge implementations.
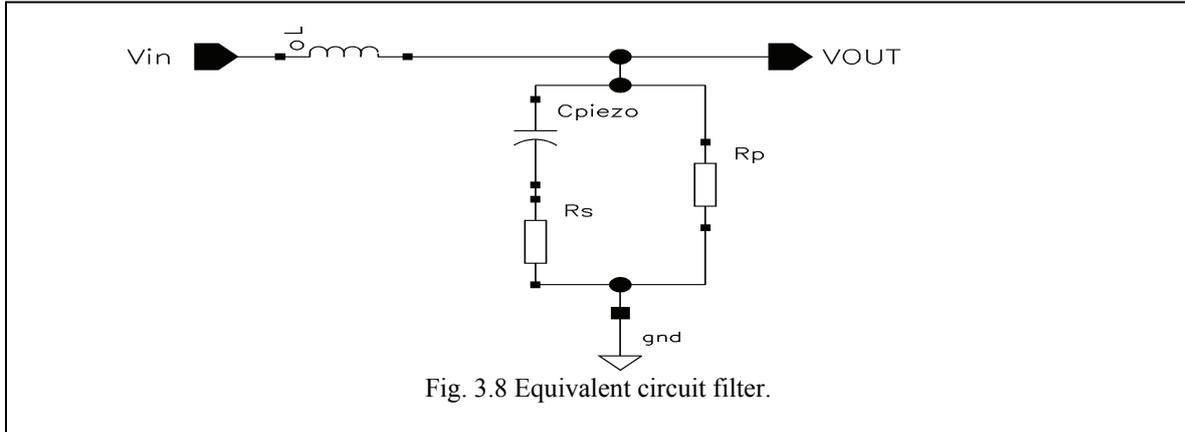
A half-bridge contains two output transistors, a high-side transistor connected to the positive power supply, and a low-side transistor connected to the negative supply. The high-side transistors can be PMOS or NMOS. The last are often used to reduce size and capacitance, but special gate-drive techniques are required to control them. Half-bridge circuits can be powered from bipolar power supplies or a single supply, but the single-supply version imposes a potentially harmful dc bias voltage, across the load.

For the piezo driver system the half-bridge topology with bipolar supplies is chosen, PMOS for the high-side transistor and NMOS for the low-side transistor. The choice of a half-bridge is made for a couple of reasons. The first reason is because only one filter is required for the half-bridge configuration and therefore fewer components outside the IC have to be used. Driving the half-bridge is less complicated because only one transistor pair has to be controlled. The feedback for the half-bridge is also less complicated. Moreover the load can for one side be connected to the ground. This forms a constant reference to ground. All these reasons ease the design for the piezo driver system.

3.2.2 Filter

Class-D amplifier must have a filter to extract, or recover, the signal from the pulsed waveform. A low-pass filter having a cut-off frequency near the highest signal frequency is used. The filter suppresses the high-frequency components of the pulse train and, in effect, recovers the average value of the pulse train. Since the average value of the pulses depends on the pulse widths, the output of the filter is a waveform that increases and decreases as the pulse widths increase and decrease. A low-pass filter also minimizes electromagnetic interference (EMI) caused by the switching of the amplifier.

A common configuration is a low-pass filter with a cut-off frequency near the highest signal frequency. The most used filter configuration for this use is an inductor (L) capacitor (C) combination. This type of filter dissipates less than a resistor capacitor combination. The LC filter does however have a resonance frequency. For most class-D amplifiers the speaker at the output damps the filters resonance. The analyses of the piezo-panel in chapter two did show that the piezo element also has a certain amount of resistance and therefore will damp the resonance.

Fig. 3.8 Equivalent circuit filter.

Instead of using a separate capacitor in the filter, the capacitive behaviour of the piezo-panel is used. The equivalent filter circuit is showed in figure (3.8). The filter consists of the coil L and the equivalent circuit for the piezo element. The circuit of figure (2.5 A) is used for the piezo-patch. The resonance part of the piezo circuit is left out for the evaluation of the filters transfer function. The leakage resistor, Rp, is quite large, so it will only affect the transfer function in the very low frequency range. Therefore, it is not important for the transfer function of the filter. The transfer function of the filter is given in equation (3.14).

$$H_{filter} = \frac{Uout}{Uin} = \frac{R_S \cdot C_{Piezo} \cdot s + 1}{L \cdot C_{Piezo} \cdot s^2 + R_S \cdot C_{Piezo} \cdot s + 1}$$

(3.14)

This network has one zero:

$$z_1 = -\frac{1}{R_S C_{Piezo}}$$

(3.15)

And two poles:

$$p_{1,2} = \frac{-R_S \cdot C_{Piezo} \pm \sqrt{R_S^2 \cdot C_{Piezo}^2 - 4 \cdot L \cdot C_{Piezo}}}{2 \cdot L \cdot C_{Piezo}}$$

(3.16)

This pole pair will result in a resonance frequency. The natural frequency corresponding to this resonance frequency is determined by the LC-interaction, see formula (3.17).
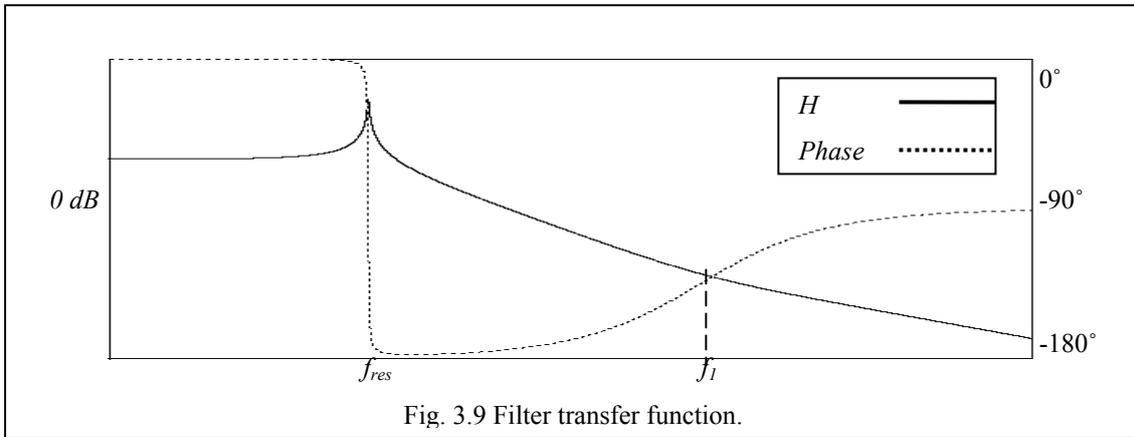
$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{Piezo}}}$$

(3.17)

At this resonance frequency (f_{res}) a peak in the amplitude characteristic occurs. The amplitude rises around this frequency and the phase angle changes from zero to 180°. For small values of Rs the cut-off frequency and resonance frequency of the filter are very close together. Formula (3.17) can therefore be used to determine the cut-off frequency.

At a certain frequency, f_1, the impedance of the capacitor becomes equal to the value of the series resistor. This is represented by the zero in the transfer function. As Rs is assumed small, this frequency is assumed to be higher than the resonance frequency. From this frequency upward, the capacitor action is negligible and the network starts to act as an LR-filter. The phase angle becomes 90°. This frequency is:

$$f_1 = \frac{1}{2\pi \cdot R_S C_{Piezo}}$$
(3.18)

The transfer function of the filter is showed in figure (3.9).

Fig. 3.9 Filter transfer function.

The highest frequency of the input signal is 500 Hz. Therefore the cut-off frequency of the output filter could be placed at that particular frequency. However, the phase requirement states a maximum of 5° phase shift at all frequencies in the bandwidth. If the cut-off frequency is placed at 500 Hz the requirement of the phase shift will not be satisfied. The requirement of a 500 Hz bandwidth and a maximum phase shift of 5° conflict each other. Allowing more phase shift is not an option because less noise will suppressed with a larger phase shift. The bandwidth of the filter has therefore to become larger. The phase function can be calculated with equation (3.19).

$$\arg\left(\frac{Uout}{Uin}\right) = \arg\left(-\frac{\frac{1}{C_{Piezo} \cdot \omega}}{R_S}\right) - \arg\left(\frac{L \cdot \omega - \frac{1}{C_{Piezo} \cdot \omega}}{R_S}\right)$$
(3.19)

The formula for the phase, (3.19), shows that the phase characteristic depends on the series resistance, Rs, in the piezo circuit model. The value of the resistance can however not be predicted. No formula has been found for the resistance of Rs, only the measured value of TNO is known. The resistance is assumed to scale with the size of the piezo element. A maximum and minimum resistance value of respectively 50 Ω and 5 Ω are taken. In the worst case scenario the piezo element has a capacitance, Cp, of 500 nF and a resistance, Rs, of 50 Ω. With the use of formula (3.19) and formula (3.17) the inductance of the coil and the cut-off fre-

quency can be calculated. With the given values for the components and phase shift, the inductance of the coil and bandwidth can be calculated. The cut-off frequency has to be placed at 628 Hz to get a 5° shift at 500 Hz. The phase shift criteria is satisfied with this bandwidth, however, a bandwidth of 628 Hz still gives a problem for the filer design.

For the 500 nF and 50 nF piezo-patches a coil of respectively 51 mH and 507 mH have to be used. These are large inductance values and require coils with large dimensions, much larger than the 6 mm of space which is available on the piezo-panel. The largest inductance value for a coil which can fit on the piezo-panel has an inductance of 3.9 mH [19]. This value is a lot smaller than the wanted coil of 507 mH. Because the inductance of the coil is smaller the bandwidth of the filter becomes larger. For the 500 nF and 50 nF piezo-patches the cut-off frequency becomes respectively 3.6 kHz and 11.4 kHz. The required bandwidth of 500 Hz can not be satisfied in this way.

Other ways to increase the inductance of the coil do not give suitable solutions to this problem. Using several coils in series to increase the inductance would require over a hundred coils. The intention was to keep the amount of components on the piezo-panel as small as possible and a hundred coils can't be considered a small amount.
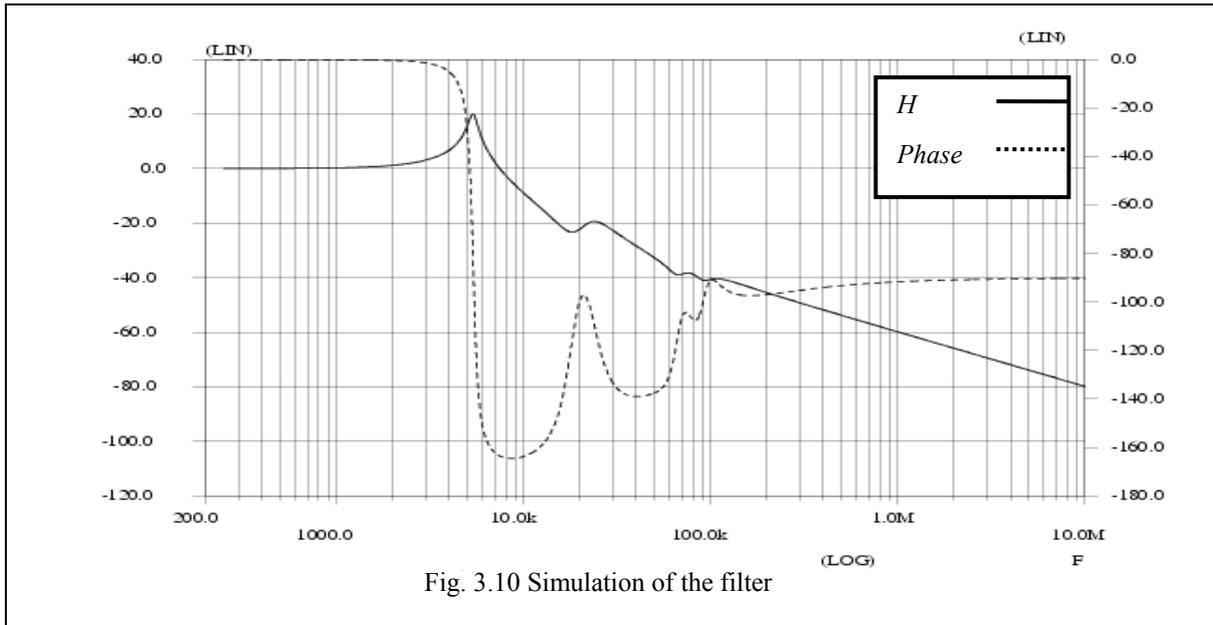Another option is to increase the capacitance in the filter. This way the bandwidth can be made smaller. But this solution comes with a price; a larger capacitance requires a larger current and thus more dissipation. The larger current also requires the use of a coil with lower inductance because a higher maximum current specification for the coil is needed. The adding of an extra capacitor also increases the resonance effects in the filters transfer behaviour. A larger peak occurs at the resonance frequency. This is not wanted because signals with that frequency will get amplified. An extra capacitor is therefore not a good solution.
Beside the use of a passive filter an active filter could be used. Replacing the inductor in a passive LC output filter with an active power buffer provides a solution for the coil problem. This approach eliminates the use of an inductor, however, active components have to be used instead. These components, transistors, operate in their linear mode. This causes high dissipation and the use of an active filter is therefore not an option.

The bandwidth of the filter has to become larger than required. Nevertheless this does not give problems for the main function of the piezo driver system. The increased bandwidth has to be taken into account for the further design of the system. The same signal requirements still have to be satisfied.
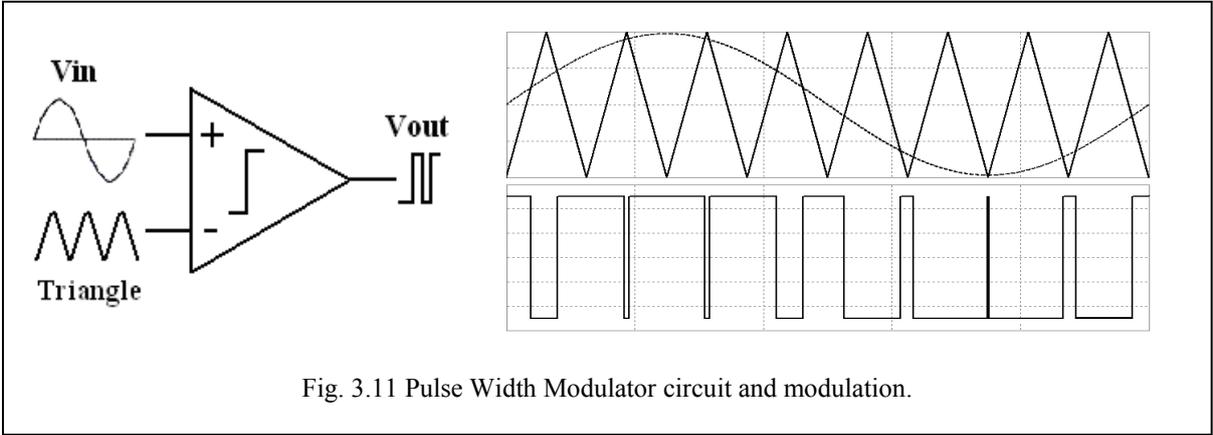
The maximum inductance available for the coil is chosen rather than a fixed bandwidth. This choice has been made because of the ripple present on the output signal. This will be explained in section 3.2.4.

The simulation of the filter's transfer function can be found in figure (3.10). The inductor has a value of 3.9 mH and the components of the equivalent piezo circuit have the same values as used in chapter 2.4, see table 2.2.

Fig. 3.10 Simulation of the filter

3.2.3 Pulse Width Modulator

Since most audio signals are not pulse trains, a modulator must be included to convert the audio input into pulses. This modulator is a fundamental component of a class-D amplifier. Various modulation schemes exist to convert the analog input signal into a pulse signal but most of them use a very similar approach. The input signal is converted to pulses; this process is accomplished by comparing a reference signal with the input signal. A circuit model of a PWM configuration can be found in figure (3.11).

Fig. 3.11 Pulse Width Modulator circuit and modulation.

For the modulation two major types of schemes exist, pulse width modulation (PWM), pulse density modulation (PD) and another form of PD, sigma delta modulation (SΔ). The last two, PD and SΔ, involve digital schemes. In the piezo driver system the input, output and feedback signal will be analog, so it is practical to choose for the analog modulation scheme (PWM).

A pulse width modulator produces a train of pulses having widths that are proportional to the level of the amplifier's input signal. When the signal level is low, a series of narrow pulses is generated, and when the input level is high, a series of wide pulses is generated, see figure (3.11).

The frequency content of the pulses includes both the desired audio signal and significant high-frequency energy related to the modulation process.

The choice of the reference signal for the pulse width modulator, indicated with *"Triangle"* in figure (3.11), is quite important in the functional design. It determines and influences the characteristics of the main system and several sub-systems. The reference signal has three important parameters; shape, frequency and amplitude.

Traditionally, pulse width modulation is categorized in two major classes by the sampling method: natural sampled PWM (NPWM) and uniform sampled PWM (UPWM). The total integrated high-frequency power in both schemes is roughly the same, since the total power in the time-domain waveforms is similar, and by Parseval's theorem, power in the time domain must equal power in the frequency domain.
However, the distribution of energy varies widely: in some schemes, there are high energy tones atop a low noise floor, while in other schemes, the energy is shaped so that tones are eliminated but the noise floor is higher. The distribution of the frequency energy is important because the amount of EMI which the amplifier produces is related with it. The EMI should be kept low, especially because the ANC system is designed to operate in airplanes.
According to the research of Nielson **[18]** the natural sampled PWM produces a favourable frequency distribution compared to the uniform sampled PWM. For a half-bridge configuration the double-sided waveform, also called triangle, gives better results than the single-sided (sawtooth). In figure (3.11) a natural sampled PWM scheme with a double-sided waveform is used for the reference signal to form the pulses.

The frequency of the reference signal has a direct impact on the dissipation of the piezo drive system. The triangle frequency determines the frequency of the pulses and with that the switching frequency of the output transistors. The dissipation caused by the switching of the transistors can be seen in formula (3.8). The switching frequency should be kept low in order to keep the dissipation low.
On the other hand the switching noise is decreased when higher frequencies are used. Higher frequencies get more attenuated by the output filter which results in lower switching noise. This effect has also consequences for the amplitude of the output ripple on the load. The output ripple, caused by the output pulses, gets more attenuated at higher frequencies. The amplitude of the ripple influences the feedback in the system. This will be discussed in section 3.2.4.

Another important aspect which determines the frequency of the reference signal is the electric behaviour of the piezo-panel and the filter. The piezo element and the filter both have resonance properties. Placing the reference signal frequency near one of the resonance frequencies could result in excessive switching noise or even oscillations. It is therefore preferred to choose a frequency which is far away from the resonance frequencies. The highest resonance frequency for the filter is at 11.4 kHz. The resonances of the piezo-panel are variable and depend on the material constants. According to chapter two the resonance peaks of the piezo-panel are very small for the higher resonance frequencies. This fact can be used to find a proper frequency for the reference signal.

The feedback loop in the system is also influenced by the switching frequency. The feedback loop will be discussed in the following section. For now it is good to know that the output signal of the filter is used for the feedback and so the choice of the reference signal frequency has also effect on the feedback. To avoid instability issues, the output signal of the filter

should have a phase shift smaller than 180˚. The transfer function of the filter, figure (3.9), shows the phase characteristic. This graph shows an 180˚ phase shift at the resonance frequency of the filter which graduate returns to a 90˚ shift. This is an important fact because for higher switching frequencies the feedback will cause no instability.

For the quality of the output signal, noise attenuation and system stability a high frequency for the reference signal is preferred. However, as discussed, the choice for a high frequent reference signal results in more dissipation. The higher dissipation can de decreased by optimizing the output transistors of the class-D design. The stability of the system is of more importance than the increase in dissipation and therefore a high frequency will be used.
At 100 kHz the resonance of the piezo-panel has still some influences on the transfer function of the output filter, see figure (3.10). At 500 kHz the resonances of the piezo-panel have no significant influence on the transfer function of the output filter. The phase shift will at that frequency be around 135°, in the worst case situation *L=3.9 mH, C_Piezo= 50 nF and Rs = 5 Ω*. This provides enough phase marge to ensure stability. However at 500 Hz the output ripple is too high which results in a low loop gain. A high loop gain is needed to suppress noise and to reduce THD. Therefore a frequency of 1 MHz is chosen for the reference signal.

The last design parameter for the reference signal is the amplitude. The input signal will be compared with the reference signal. When amplitude of the input signal is larger than the amplitude of the reference signal, clipping of the PWM occurs and signal information is lost. The reference must have larger amplitude than the maximum amplitude of the input voltage. The minimum amplitude for the reference signal is ± 1 Volt. The gain of the PWM output stage can be expressed as:

$$G_{PWM} = U_{SUPPLY} \cdot \frac{U_{Signal}}{U_{Reference}} \tag{3.20}$$

For a maximum gain of the system the amplitude of the reference signal has to be as small a possible. The amplitude of the reference is therefore chosen at 1 Volt.

3.2.4 Feedback

The feedback in the system reduces distortion and power supply noise on the output signal. Distortion of the output signal is mainly caused by nonlinearities. These include nonlinearities in the modulation technique and the dead time used in the output stage to solve the shoot-through current problem.
Information about the audio signal level is generally encoded in the widths of the Class D modulator output pulses. Adding dead time to prevent output stage shoot-through currents introduces a nonlinear timing error, which creates distortion at the speaker in proportion to the timing error in relation to the ideal pulse width. The shortest dead time that avoids shoot-through is often best for minimizing distortion.
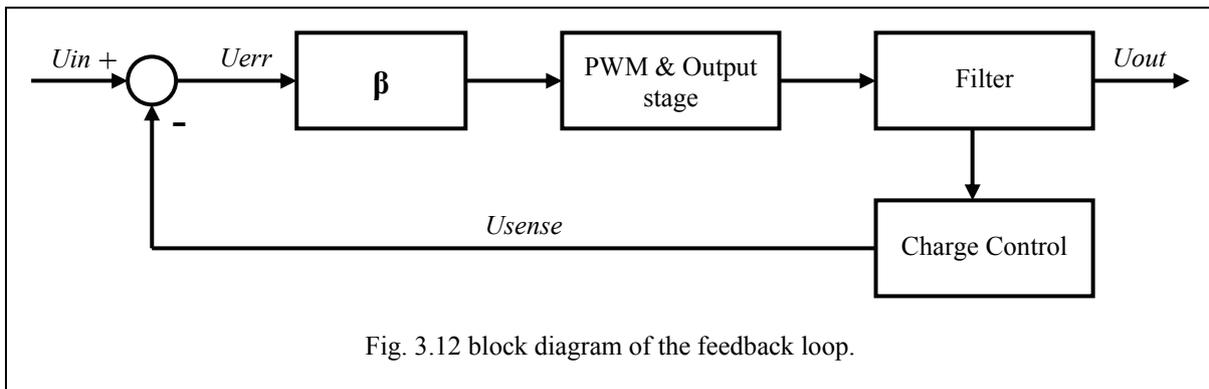Other sources of distortion include: mismatch of rise and fall times in the output pulses, mismatch in the timing characteristics for the output transistor gate-drive circuits, and nonlinearities in the components of the LC low-pass filter.

Power-supply noise couples almost directly to the speaker with very little rejection. This occurs because the output-stage transistors connect the power supplies to the low-pass filter

through a very low resistance. The filter rejects high-frequency noise, but is designed to pass the audio frequencies, including noise.

If neither distortion nor power supply noise issues are addressed, it is difficult to achieve a low total harmonic distortion and good power supply rejection (PSR). Even worse, the THD tends to be the bad-sounding high-order kind [14]. Fortunately, there are good solutions to these issues. As said, using feedback with high loop gain helps a lot. Feedback from the LC filter input will greatly improve PSR and attenuate all non-LC filter distortion mechanisms. LC filter nonlinearities can be attenuated by including the load in the feedback loop. Feedback complicates the amplifier design because loop stability must be addressed.

Applying feedback in a system increases the accuracy and decreases the noise and non-linearity in the system. The scale of improvement depends on the loop gain, the higher the loop gain the better the improvement of the systems quality [14]. The feedback system looks as shown in figure (3.12). As can be seen an extra element β is added into the loop. This element is an amplifier which is used to increase the loop gain. Besides the amplifier another important function is implemented into the feedback system. This function is represented by the *Charge Control* block. The function of this sub-functions will be discussed in the following.

Fig. 3.12 block diagram of the feedback loop.

Hysteresis behaviour of the piezo element forms a problem for the system. This problem has to be taken into account in the design of the piezo driver. The hysteresis phenomenon is well documented and several methods exist to compensate for it. Some control systems approaches have been used for overcoming the hysteresis of the piezoelectric stack actuator. One study [6] incorporates an inverse model into the systems feedforward loop to linearize the actuator behaviour. Another study [6] uses a similar approach, except that a proportional-integral-derivative (PID) controller is added in a feedback loop.
An alternative method of overcoming the hysteresis of the actuator is to use charge instead of voltage control. Electrically, the piezoelectric actuator behaves as a nonlinear capacitor, with the principal nonlinearity being a hysteresis in the charge-voltage characteristic. This electrical nonlinearity results from the same dielectric hysteresis as the electromechanical nonlinearity. Thus, it happens that the relationship between the mechanical displacement of the actuator and the applied charge is roughly linear. Hence, charge control is advantageous to the linear operation of the actuator. Literature [6], [20] show that the actuator hysteresis is reduced considerably and allows a linear relationship between the input voltage and the actuator displacement.

To overcome the problems of hysteresis charge control will be used in the piezo driver system. The charge control will be incorporated into the feedback. This control circuit has to be
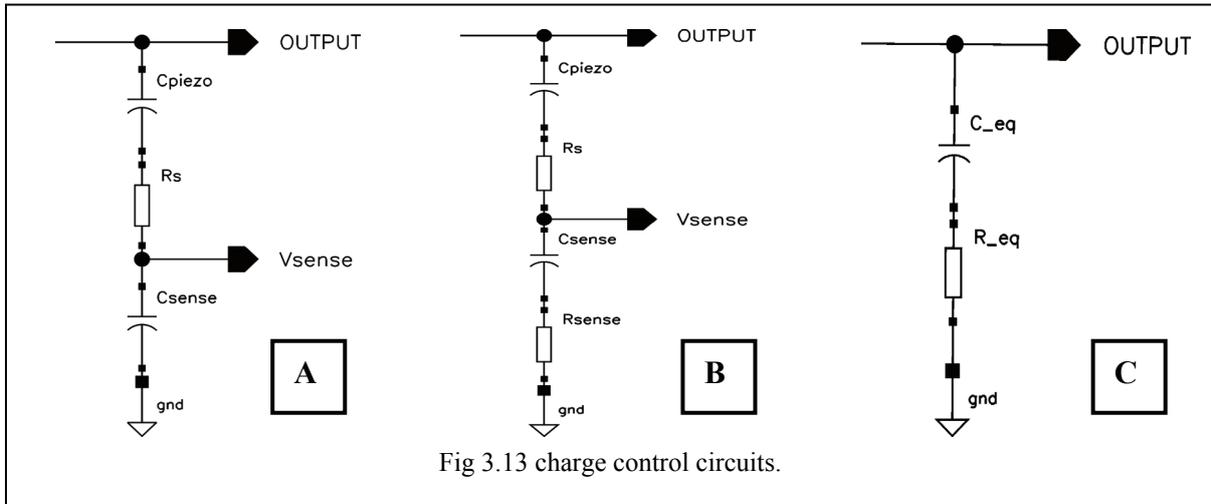
placed, in the electric circuit, in series with the piezo element for a correct function. The charge control consists of a capacitor which is placed in series with the piezo element. This capacitor will be referred as 'sense capacitor' and the charge control will also be called 'sense network'. The sense network contains in this stage only the sense capacitor.

The charge inside a capacitor depends on the capacitance of the capacitor and the applied voltage, see formula (3.21).

$$Q_{capacitor} = C_{capacitor} \cdot U \qquad (3.21)$$

The sense capacitor will be placed in series with the piezo element as can be seen in figure (3.13A). The amount of charge inside the sense capacitor is the same as in the piezo element. This can be understood by looking at the current. The current through the branch, piezo element and sense network, is for all components the same. By definition the current can be expressed as charge per second, see equation (3.22).

$$I = \frac{Q}{s} \qquad (3.22)$$

So when the current for both components is the same then it can be proven that the charge will also be the same in the piezo element and sense capacitor. This fact is used together with formula (3.21) to find a linear expression for the charge inside the piezo element. The voltage over the sense capacitor can be used as charge control signal in the feedback loop.

Fig 3.13 charge control circuits.

The piezo element and the sense capacitor together form a voltage divider. The voltage is divided over the two capacitors, this means that the sense capacitor decreases the maximum voltage drop over the piezo element.

$$U_{SENSE} = \widehat{U}_{OUTPUT} \cdot \frac{C_{PIEZO}}{C_{SENSE} + C_{PIEZO}} \qquad (3.23)$$

However, the input signal has maximum amplitude of 1 Volt, so 1 Volt for the feedback signal will be sufficient. This leaves the greater part of the supply voltage left for the driving of the piezo element. The voltage over the sense capacitor can be calculated with formula (3.23).

With a maximum output voltage of the supply voltage and 1 volt for the sense signal, the capacitance of the sense capacitor can be calculated with equation (3.24).

The sense capacitor has to be adapted to the capacitance of the piezo in order to get the wanted voltage drop over the sense capacitor. For a supply voltage of 60 Volt and the maximum capacitance of 500 nF for the piezo-panel, the sense capacitor becomes 29.5 µF.

$$C_{SENSE} = C_{PIEZO} \cdot \left(\frac{\hat{U}_{OUTPUT}}{U_{SENSE}} - 1 \right) \qquad (3.24)$$

This to large to integrate on chip and has therefore to be placed outside the chip. This means that another component must be placed on the piezo-panel. However, the sense capacitor has to be adapted to the capacitance of the piezo element and hence must be a variable component.

The charge control circuit can not function correctly in the feedback loop when only the sense capacitor is used in the sense network. The phase characteristic of the sense network has a 180° phase shift at the resonance frequency of the filter and stays at 180° for the rest of the frequency spectrum. Applying this signal into the feedback loop will result in an instable system. This can be solved by adding a resistor in series with the sense capacitor, see figure (3.13B). The series resistor in the sense network causes the phase to return to 90° at higher frequencies.

The transfer function of the sense network with the sense resistor, *Cs + Rs*, can be seen in figure (3.14). The simulation shows the transfer function of the filter with the added charge control circuit. The input is applied to the input of the filter and the *V(sense)* is used as the output signal, see figure (3.13B).
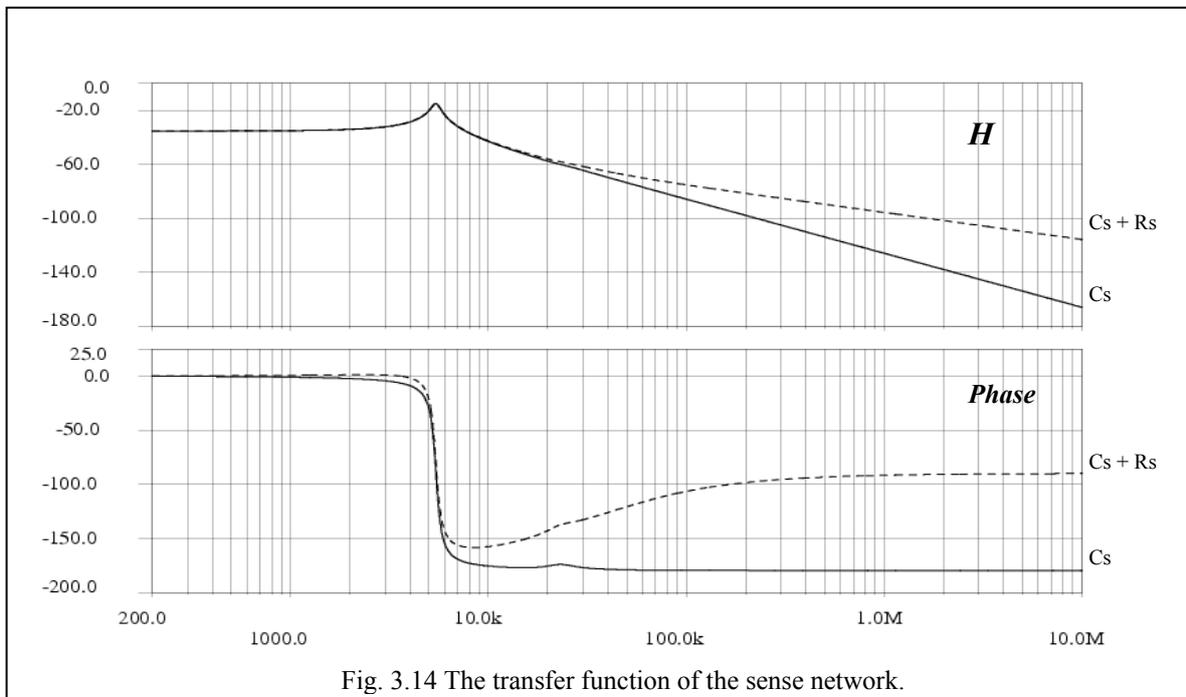

Fig. 3.14 The transfer function of the sense network.

Another advantage of adding the resistor to the sense network is that this circuit can be designed with the same frequency dependent properties as the piezo model. This way the voltage ratio of the piezo-panel and sense network becomes frequency independent.

To achieve this, the resistors in the sense network, *Rsense*, has to be chosen in such a way that the time constants (*RC*-time) of both models are equal. With the use of equation (3.24) and equation (3.25) the formula for *Rsense* (3.26) can be found.

$$R_{S,Piezo} \cdot C_{Piezo} = R_{SENSE} \cdot C_{SENSE} \tag{3.25}$$

$$R_{SENSE} = R_{S,Piezo} \cdot \left(\frac{\widehat{U}_{OUTPUT}}{\widehat{U}_{SENSE}} - 1 \right)^{-1} \tag{3.26}$$

Adding of the sense resistor does not influence the charge control. The current through the branch, piezo element plus the sense circuit, is for all components the same. Thus the charge in the sense capacitor is still the same as in the piezo element.

The load of the system is formed by the piezo element and the sense network. Since the time constants of the piezo and the sense network are designed equal, the resistors and capacitor can be taken together. By doing this, the figure (3.13B) can even be simplified into figure (3.13C). The sense network has no influences on the transfer function of the filter when the time constants of the piezo model and sense network are the same. The equivalent resistor and capacitor value for the simplified circuit can be calculated with the following equations.

$$R_{Eq} = R_{S,Piezo} + R_{SENSE} \tag{3.27}$$

$$C_{Eq} = \frac{C_{PIEZO} \cdot C_{SENSE}}{C_{PIEZO} + C_{SENSE}} \tag{3.28}$$

The simplification of the piezo element and sense network can be used to simplify the transfer function of the piezo driver system. The filter's transfer function can be found with formula (3.14). The charge control can be described as an attenuation or gain, equation (3.29).

$$A_{SENSE} = G_{SENSE}^{-1} = \frac{\widehat{U}_{OUTPUT}}{\widehat{U}_{SENSE}} \tag{3.29}$$

With the maximum output amplitude and the sense signal amplitude of respectively 60 Volt and 1 Volt, the sense network gives an attenuation of 60.
The gain for the piezo driver with feedback is found with formula (3.30). The gain of the PWM and output stage of the design is given in equation (3.20). The filter has a gain of 1 for signals in the bandwidth of the filter. The gain of the sense network has just been calculated and given above in formula (3.29). The gain β of the loop amplifier is not determined so far.

$$G_{PDS} = \frac{G_{\beta} \cdot G_{PWM} \cdot H_{FILTER}}{1 + G_{\beta} \cdot G_{PWM} \cdot H_{FILTER} \cdot G_{SENSE}} \tag{3.30}$$

The loop amplifier is essential to decrease noise and distortion of the output signal. Without it the piezo driver system is not able to produce the maximum output signal. This can be seen when the available gains of the different sub-functions are entered into equation (3.30). The gain of β is taken as 1 for now. The gain of the filter is also 1 when the input signal frequency bandwidth is assumed.

The PWM has a gain of 60 and the sense network an attenuation of 60. With these numbers the loop gain becomes:

$$G_{PDS} = \frac{1 \cdot 60 \cdot 1}{1 + 1 \cdot 60 \cdot 1 \cdot \frac{1}{60}} = \frac{60}{2} \tag{3.31}$$

In this way only half of the maximum output voltage can be attained. To get the maximum output voltage the β amplifier should have a theoretical gain of infinity. This is of course not possible however a high gain can be achieved.

As discussed a higher loop gain results in reduction of noise and distortion. According to **[21]** the influences of noise and distortion acting on the output are decreased as:

$$\frac{C}{S} = \frac{1}{1 + H_L} \tag{3.32}$$

Where C stands for the influence signal acting at the output, S stands for the noise and distortion at the output and H_L for the loop transfer function. For a high loop gain the influence of the noise and distortion acting on the output signal become small. A high loop gain helps therefore by the reduction of noise and distortion at the output.

The gain of the β amplifier is however limited by triangular waveform on the output. This triangle on the output is caused by the switching of the output stage. When feedback is applied, the sense signal (U_{SENSE}) is subtracted from the input signal (U_{IN}), see figure (3.12). The high-frequency triangle is therefore also present in the error signal (U_{ERR}) and is amplified by the β amplifier. The PWM compares the error signal with the reference signal which has also a triangular waveform.

The output of the PWM changes polarity when the triangles cross each other. In order for this process to work correctly, the amplitude of the reference triangle should be larger than the amplitude of the error triangle or, more accurately, the slopes of the reference triangle should be steeper than those of the error triangle **[17]**. When the error signal has a steeper slope than the reference signal then unnecessary switching of the output stage occurs. This effect can happen several times within a the reference triangle period, creating many small switching peaks, see figure (3.15). Although this behaviour does not cause instability of the amplifier function, it increases the switching frequency which results in extra energy consumption of the driver electronics.

The slew rate of the error signal is mainly influenced by the β amplification factor, provided that the other gain factors have already been chosen.

The triangle or ripple on the output depends on the switching frequency, the supply voltage and the attenuation of the filter. The amplitude of the triangle can be calculated as follows. The output filter consists of the inductor,
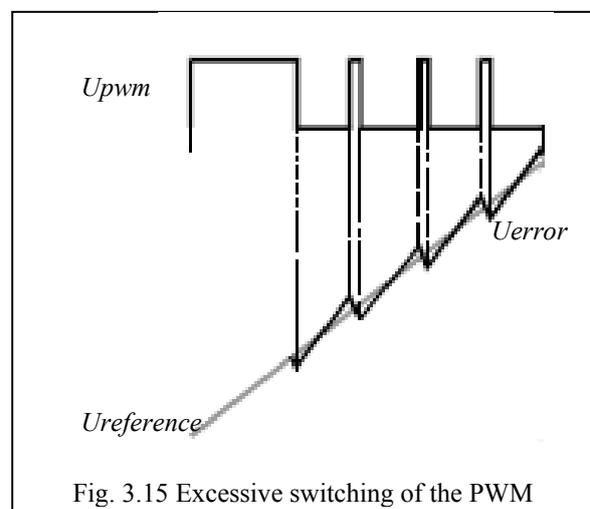

Fig. 3.15 Excessive switching of the PWM

the capacitor and resistors of figure (3.8). The parallel resistor is left out of the calculation because this component has only influence at low frequencies. The series resistor is the equivalent resistor of equation (3.27). The switching frequency is chosen at 1 MHz as discussed in section 3.2.3. At this frequency the capacitor in the output filter can be neglected. For the calculation the circuit consists of the inductor and series resistor. According to **[22]** the ripple current can be approximated by formula (3.33).

$$\hat{i}_{Ripple} = \frac{U_{SUPPLY} - \overline{U}_R}{L} \cdot d \cdot T_C \qquad \text{if} \qquad T_C \langle\langle \tau \qquad (3.33)$$

$$\tau = \frac{L}{R_{eq}} \qquad (3.34)$$

In these formulas U_{SUPPLY} stands for the supply voltage, $\overline{U}_R$ stands for the average voltage over the load resistor R_{eq}, d stands for the duty-cycle and T_C for the switching period. The ripple on the feedback signal *Usense* can be found with (3.35).

$$\widehat{U}_{Ripple} = R_{SENSE} \cdot \hat{i}_{Ripple} \qquad (3.35)$$

The largest ripple occurs when the duty-cycle is 50%. The average voltage over the load resistor is 0 Volt since the positive and negative pulses have the same time duration with this duty cycle. The supply voltage is again 60 Volt. The resistance of R_{eq} is calculated with formula (3.26) and (3.27). The switching frequency is 1 MHz and the switching period is thus 1 µs. The maximum inductance of 3.9 mH is used for the calculation of the ripple current. This current can now be found:

$$\hat{i}_{Ripple} = \frac{60V - 0V}{3.9\,mH} \cdot 0.5 \cdot 1\,\mu s = 7.7\,mA \qquad (3.36)$$

The series resistance of the piezo element will in the worst situation be 50 Ω, provided that the inductor and voltage supply are not changed. The sense resistor is approximated with the 50 Ω and with this the maximum ripple on the sense signal can be calculated. The maximum ripple will be:

$$\widehat{U}_{Ripple} = \frac{50\,\Omega}{60 - 1} \cdot 7.7\,mA = 6.5\,mV \qquad (3.37)$$
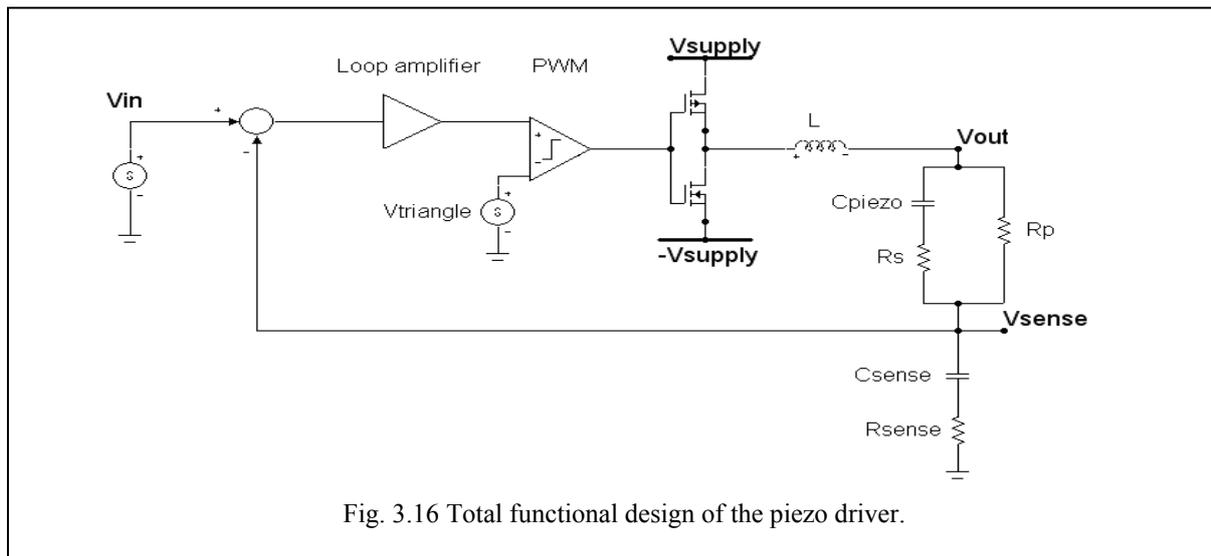
The same ripple is present on the error signal which gets amplified by the loop amplifier β. With the maximum voltage ripple the gain of the loop amplifier can be calculated. Both the reference signal of the PWM and the voltage ripple have a period of 0.5 µs. The maximum allowed gain is determined by the slope of the ripple. The ripple can have a maximum slope equal to the slope of the reference triangle of the PWM. The gain of the loop amplifier can at the very most be:

$$G_\beta = \frac{\widehat{U}_{triangle}\big/\tfrac{1}{2} \cdot T_C}{\widehat{U}_{Ripple}\big/\tfrac{1}{2} \cdot T_C} = \frac{2V}{6.5\,mV} = 308 \qquad (3.38)$$

To have some room for error the gain of the loop amplifier β should be chosen smaller than the maximum allowed gain.
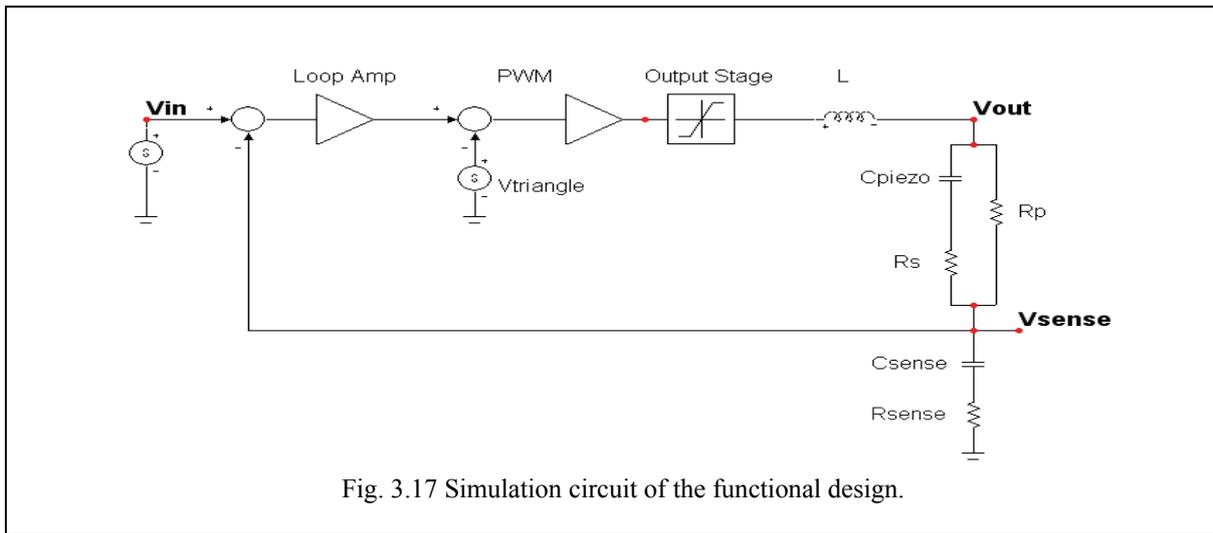
3.3 Total functional design

All the important aspects in of the design of the piezo driver system have been discussed. The total functional design of the piezo driver can be seen in figure (3.16).

Fig. 3.16 Total functional design of the piezo driver.

For the several sub-functions certain design choices and calculations have been made. The most important numbers are summarized in the following.

Class-D
- Output voltage of ±60 Volt
- Gain of 60

PWM reference signal
- Triangular
- 1 Volt amplitude
- 1 MHz

Filter
- Inductor 3.9 mH
- Capacitor 50 nF – 500 nF (piezo element)

Feedback
- Csense = Cpiezo * 59
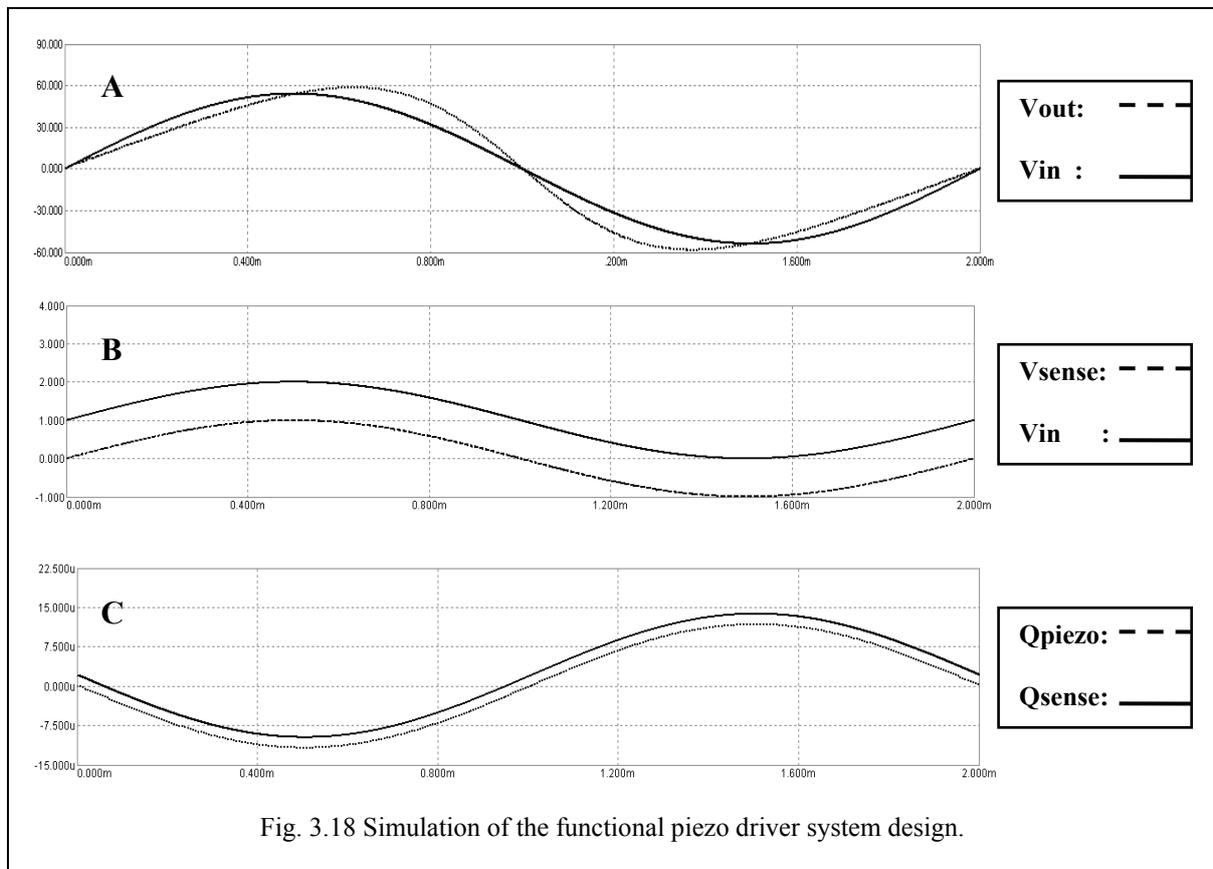- Rsense = Rs / 59
- Loop amplifier max. gain of 308

Simulation of the functional design is done as a proof of concept. This simulated circuit is showed in figure (3.17). The simulation is done with *micro-cap* using only ideal functional blocks. The PWM and output stage are simulated using a subtractor, amplifier and a voltage limiter. The reference triangle is subtracted from the amplified error signal. This gives a signal which is positive when the error signal is larger than the reference triangle and a negative voltage vice versa.

Fig. 3.17 Simulation circuit of the functional design.

The positive or negative voltage is amplified with a very high gain. The last block limits the voltage to 60 Volt and -60 Volt. This simulates the output pulses from the class-D output stage.

The piezo-panel is modelled with the circuit of figure (2.5A). These components have the same value as used in table (2.2) with the total capacitance of 223 nF. To simulate the nonlinear behaviour of the piezo-panel, the piezo capacitance (*Cpiezo*) is made variable by using a nonlinear capacitor in *microcap*. The sense network is adapted to piezo element using formula (3.24) and (3.26) for the sense capacitor and sense resistor respectively.

The simulation can be seen in figure (3.18).

Fig. 3.18 Simulation of the functional piezo driver system design.

The top graph shows the output voltage and the input voltage, indicated with respectively *Vout* and *Vin* in figure (3.18A). The output voltage is not a perfect sinus wave as can be seen. This is because of the nonlinear capacitance of the piezo. However the system is charge controlled. The third (fig. 3.18C) graph shows the charge inside both capacitors. This graph is obtained by integrating the current through the capacitors. The sense line is increased with 2 μC to clearly see that both graphs are equal. The charge in the piezo is equal to the charge in the sense capacitor.

The sense signal (*Vsense*) shows a nice sinusoidal signal which is similar to the input signal (*Vin*), see figure (3.18B). In the graph the input signal is increased with 1 Volt to be able to show the similarity between *Vsense* and *Vin* .

The charge control function works and the functional design shows good results. The phase shift and THD of the system can not be evaluated because the functional design is simulated with ideal components.

The next step is to convert the functional blocks to an integrated circuit. This will be done in chapter four.

4. Circuit implementation

In this chapter the several sub-functions needed for the piezo driver are translated to circuit designs which can be integrated on chip. The functional blocks are converted to transistor schematics and component values are adapted for IC design.

The design of the IC makes use of the silicon-on-insulator (SOI)-based technology called A-BCD. This technology allows creating low voltage and high voltage circuits on the same wafer without latch-up phenomena. This way a 60 Volt output stage can be realized on the same wafer as the 12 volt internal circuitry.

The output stage of the piezo driver uses high voltages therefore DMOS transistors are necessary for this part. The three types of DMOSTs used are low voltage DMOS (lv_DMOS), high voltage DMOS (hv_DMOS) and extra high voltage DMOS (ehv_DMOS) which can withstand drain-source voltages of 12 V, 60 V, and 120 V respectively.
The other sub-functions do not require the use of DMOS transistors. They are realised with normal MOSTs. The supply voltage for these blocks is chosen at 2.5 V and -2.5 V to obtain low dissipation for the piezo driver.

The different blocks which are required on chip can be seen in figure (4.1). Except for the power supply and circuit protection block all function blocks are designed.
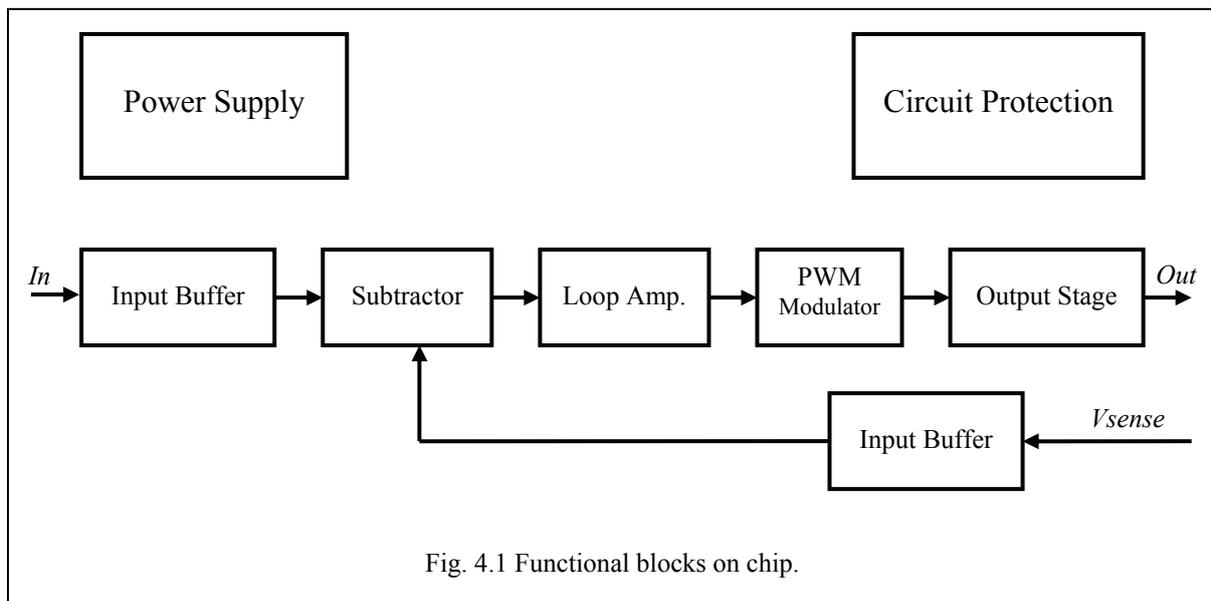

Fig. 4.1 Functional blocks on chip.

The power supply provides the different supply and bias voltages for the functional blocks. The bias current for the current mirrors in the designs are generated as well in the power supply. The supply voltages needed for the output stage are 60 Volt and 48 Volt, positive and negative. The low voltage circuits use a supply voltage of plus and minus 2.5 Volt. As indicated, the power supply will not be designed. Instead ideal voltage and current sources are used. This decision is made because the power supply is assumed to be a standard circuit and therefore does not have to be configured for the piezo driver system.

The circuit protection block monitors the system and protects the system from destroying it-self. This block consists out of several circuits which all safeguard the system from certain system failures.

The dissipation of class-D's output stage, though lower than that of linear amplifiers, can still reach levels that endanger the output transistors if the amplifier is forced to deliver very high power for a long time. To protect against overheating due to ambient temperature, tempera-ture-monitoring control circuitry is needed.

Excessive current flow in the output transistors is another dangerous situation. The low on resistance of the output transistors is not a problem if the output stage and load terminals are properly connected, but enormous currents can result if these nodes are inadvertently short-circuited to one another, or to the positive or negative power supplies. If unchecked, such cur-rents can damage the transistors or surrounding circuitry. Consequently, current-sensing out-put transistor protection circuitry is needed.
Most switching output stage circuits work well only if the positive power supply voltages are high enough. Problems result if there is an under-voltage condition, where the supplies are too low. Therefore protection against under-voltage is also needed.

The protection circuits are needed when an actual chip is made. They however are not re-quired for the primary function of the piezo driver system. So the protection circuit block will not be designed.

The design of the different functional blocks will be discussed in the following sections. The piezo driver input signal is followed through the system and along the way the functional blocks in this path will be discussed. The discussion starts with the input buffer and ends with the output stage.

4.1 Input Buffer

The piezo driver uses two input signals which are coming from outside the chip. To prevent the circuits inside the chip from loading the circuits outside the chip and vice versa a buffer is used. The interposed buffer amplifier prevents the second circuit from loading the first circuit unacceptably and interfering with its desired operation. A voltage follower is used to copy the input voltage one on one to the output, see fig-ure (4.2).
A buffer may be constructed very simply by connecting the output of an operational ampli-fier to its inverting input (negative feedback), and connecting a signal source to the non-inverting input. For this circuit, the output volt-age is simply equal to the input voltage. The input impedance of the op-amp is very high, meaning that the input of the op-amp does not load down the source or draw any current from it. Because the output impedance of the op-amp is very low, it drives the load as if it were a per-fect voltage source.
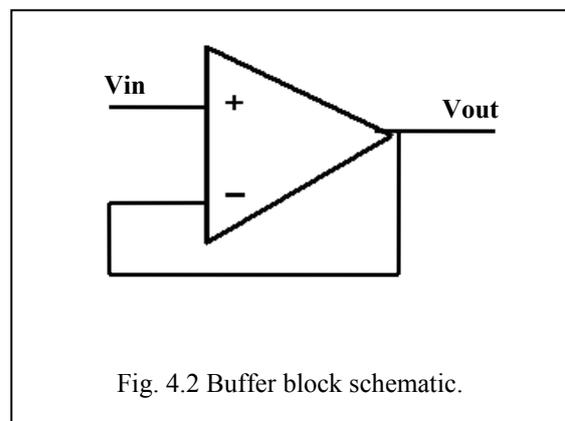

Fig. 4.2 Buffer block schematic.

For the realisation of the buffer an opamp design is needed. Because the opamp will be used in the realisation of other sub-functions as well, it will be discussed into further detail in this section.

The op-amp which is needed for the design of the several sub-functions must have a high gain, output swing at least as large as 1 Volt, low dissipation and low output impedance. To accomplish this, a two stage operational amplifier with output stage will be designed.
The first stage of the amplifier provides a high gain and the second stage large swings. A two stage configuration isolates the gain and swing requirements. Each stage in figure (4.3) can incorporate various topologies. The circuit design is also shown in appendix VII.
The second stage is configured as a simple common-source stage so as to allow maximum output swings [23]. To obtain a higher gain, the first stage is implemented as an OTA.
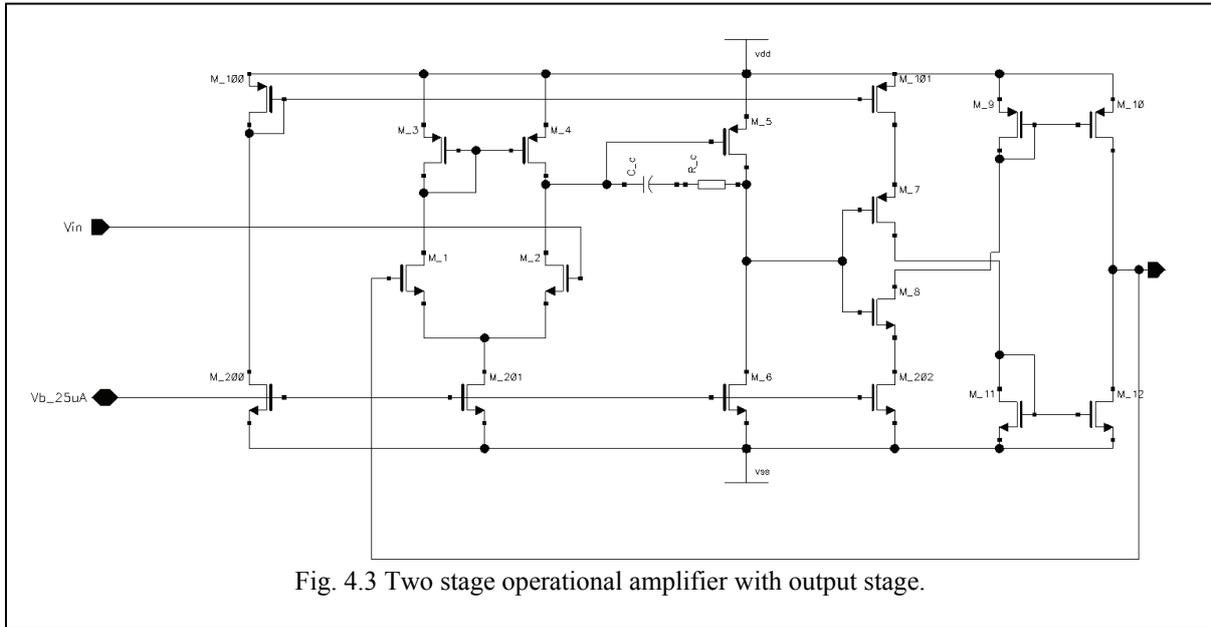

Fig. 4.3 Two stage operational amplifier with output stage.

The first stage consists of a OTA converting the differential input voltage to currents. This is accomplished by transistors *M1* and *M2* in figure (4.3). These currents are applied to a current-mirror load (*M3* and *M4*) recovering the voltage. The transistor (*M5*) of the second stage converts the second-stage input voltage to current. This MOST is loaded by a current-sink load, which converts the current to voltage at the second-stage output. This two-stage op-amp is a widely used topology [24].
The two stages are biased with a low current to minimize the dissipation. The current mirror is biased at 50 µA, *M100* and *M200*.
The gain of the first stage and second stage can be calculated with respectively formula (4.1) and formula (4.2).

$$G_{stage\,1} = gm_{1,2} \cdot \left[\left(r_{O2} \right) // \left(r_{O4} \right) \right] \tag{4.1}$$

$$G_{stage\,2} = -gm_5 \cdot \left[\left(r_{O5} \right) // \left(r_{O6} \right) \right] \tag{4.2}$$

Where,

$$r_{0\,M} \approx \frac{1}{\lambda_M \cdot Id_M} \tag{4.3}$$

The output stage is added to obtain a lower output resistance. The transistors *M7* and *M8* work as an inverter pair which pinch off the current sources *M101* and *M202*. When the gate voltage of *M7* and *M8* rise then the drain current of these transistors decrease and increase respectively. The current mirror of *M9* and *M10* amplifies the drain current of *M8*. The same goes for the current mirror *M11* and *M12*, they copy the drain current of *M7*. The difference between the current of *M10* and *M12* gives the output current. The drain currents can be as high as 350 µA. This is low current is chosen to obtain low dissipation in the circuits. It has however consequences for the output resistance. The output impedance of the output stage can be approximated by equation (4.5).

$$R_{OUT} = r_{0M10} \, // \, r_{0M12} \tag{4.5}$$

Very low values for the output resistance can not be attained in this way, however applying feedback reduces the output resistance. Still the output resistance of the op-amp has to be taken into account with the design of all the circuits. The load resistance should be taken high to avoid influences of the op-amp's output resistance.

The output voltage at the output stage can approximately be as high as the positive supply voltage and as low as the negative supply. For large $\left(\frac{W}{L}\right)$ values for *M9*, *M10*, *M11* and *M12* the voltage swing can be approximated by:

$$Vss \leq Voutput \leq Vdd \tag{4.6}$$

For the calculation of the output stage gain, the circuit is assumed to be symmetrical. This means that gm and impedance of the part which is made up from *M7*, *M11* and *M12* is equivalent to the other part of the output stage consisting of *M8*, *M9* and *M10*. This is used in the small signal equivalent circuit of the output stage to find an expression for the gain. The transistors *M101* and *M202* are not taken into account in this expression. The gain can be described formula (4.7A) which can be simplified to (4.7B)

$$G_{output} = 2 \cdot \left(r_{0M10} \, // \, r_{0M12}\right) \cdot \left(r_{oM7} \, // \, r_{0M11}\right) \cdot \frac{gm_7 \cdot gm_{12}}{1 + gm_{11} \cdot \left(r_{0M7} \, // \, r_{0M11}\right)} \tag{4.7A}$$

$$G_{output} = 2 \cdot \left(r_{0M10} \, // \, r_{0M12}\right) \cdot gm_7 \frac{(W/L)_{M12}}{(W/L)_{M11}} \tag{4.7B}$$

Where assumed,

$$gm_{11} \cdot \left(r_{0M7} \, // \, r_{0M11}\right) \gg 1$$

The total gain of the operational amplifier can now be found with the equations (4.1), (4.2) and (4.7).

$$G_{opamp} = G_{stage1} \cdot G_{stage2} \cdot G_{output} \tag{4.8}$$

The gain expressions are used in the design of the circuits. Transistor sizes are calculated and adapted in order to get a high gain. The op-amp configuration must have a high gain for good

functionality. The total gain of the designed circuit is checked with formula (4.8) and is designed with a gain of 5000.

The operational amplifier is used in a negative feedback configuration. In this way, the relatively high, inaccurate gain can be used with feedback to achieve a very accurate transfer function that is a function of the feedback elements only. However, it is very important that the signal fed back does not cause instability. To prevent instability the transfer function of the op-amp has to be compensated.

The compensation method used is the 'Miller' compensation technique [23], [24]. This technique is applied by connecting a capacitor, Cc in figure (4.3), from the output to the input of the second stage. This moves the poles of the op-amp to a new location. It however also creates a right half-plane zero. The right half-plane zero tends to limit the gain bandwidth of the op-amp. There are several ways of eliminating the effect of this zero. One approach is to eliminate the effect of the zero through the insertion of a nulling resistor, Rc, in series with Cc.

This compensation technique is used to control the phase shift in the feedback loop of the piezo driver. The total shift has to be adjusted to insure a stable system.
The buffer is designed as showed in figure (4.3) with the discussed op-amp configuration. The transient simulation of the designed buffer is shown in figure (4.4). The maximum values which can be expected for the input signal are used, 1 Volt amplitude at 500 Hz. The buffer shows a precise copy of the input signal.
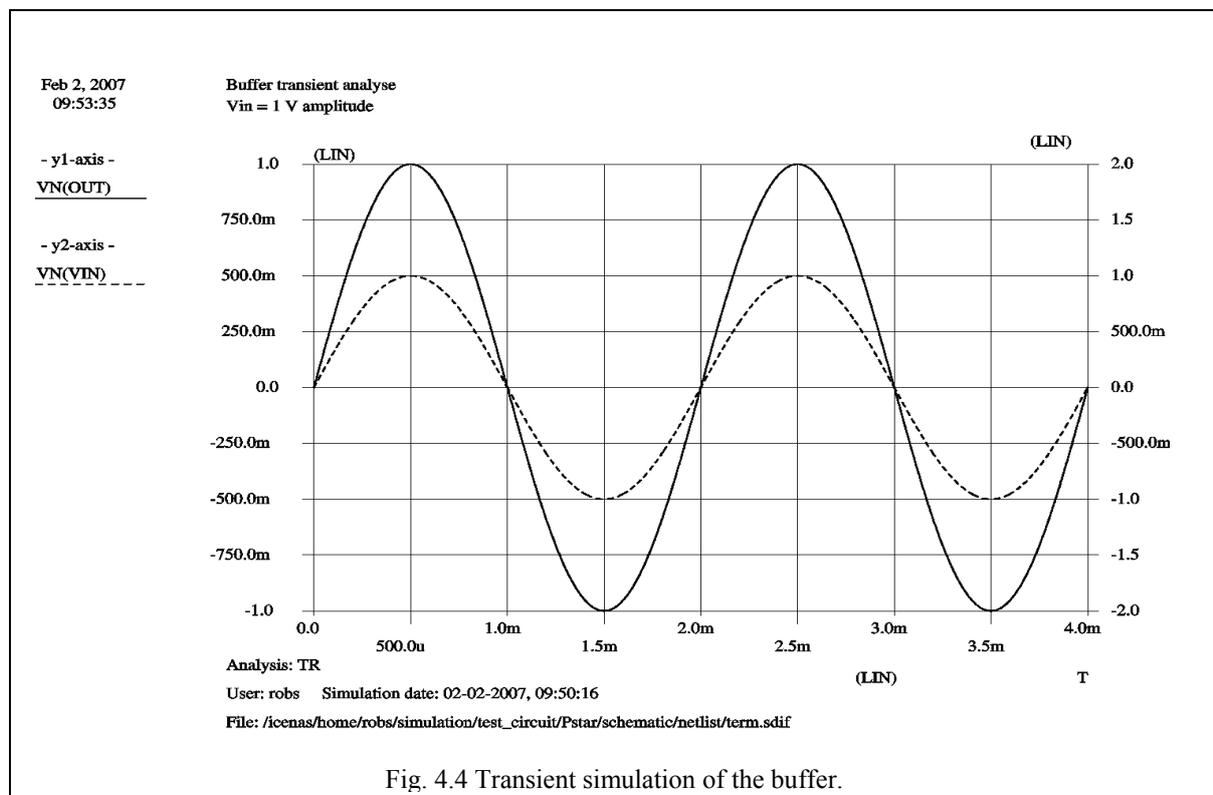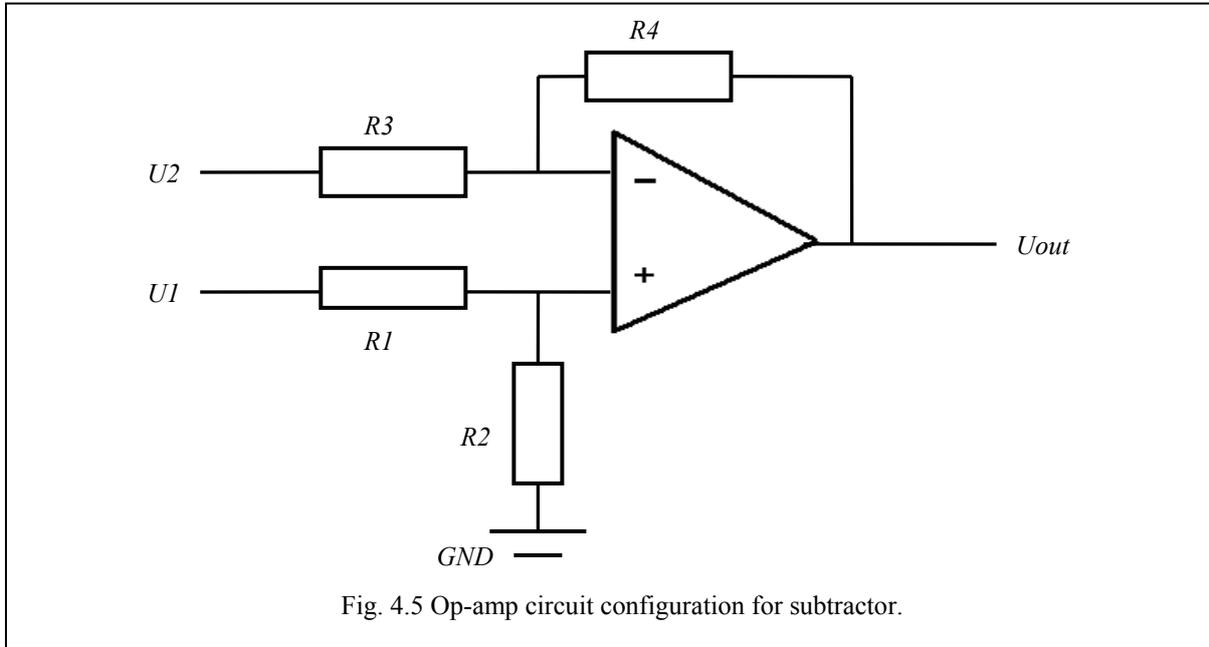

Fig. 4.4 Transient simulation of the buffer.

4.2 Subtractor

The subtractor is used in the feedback loop of the piezo driver to subtract the feedback signal from the piezo driver's input signal. This provides the error signal which is used to adjust the output of the piezo driver. The subtractor can be realised with the use of an op-amp **[13]**. The op-amp circuit can be seen in figure (4.5).

Fig. 4.5 Op-amp circuit configuration for subtractor.

The output of the subtractor can be described with equation (4.9).

$$U_{OUT} = \left(\frac{R_3 + R_4}{R_3}\right) \cdot \left(\frac{R_2}{R_1 + R_2}\right) \cdot U_1 - \left(\frac{R_4}{R_3}\right) \cdot U_2 \qquad (4.9)$$

When all resistors are chosen with the same resistance, the output function of the subtractor simplifies to *Uout = U1 - U2*.

The same two stage op-amp topology is used for the design of the subtractor. For a proper function of the circuit the op-amp has to have a high gain and low output resistance. If not the subtraction of the two signals will be less accurate. This results in a less accurate amplification of the input signal. The output stage is slightly altered to get lower dissipation while having a low output resistance, an class-AB configuration is used **[24]**. The circuit design of the subtractor is illustrated in figure (4.6). In appendix VIII an enlarged circuit design is showed.

The bias current can be determined by the voltages at the gates of *M9* and *M10*. When the input is taken positive, the current in *M7* increases, it is mirrored as an increasing current in *M11*, which provides the sinking capabilities for the output current. When the input is decreased, *M8* can source output current.

The feedback resistors in the subtractor design are taken quite large to minimize the effect of the op-amp's output resistance. All the resistors have the same value to get one on one relation between the output of the subtractor and the difference between the piezo driver input signal and the feedback signal.
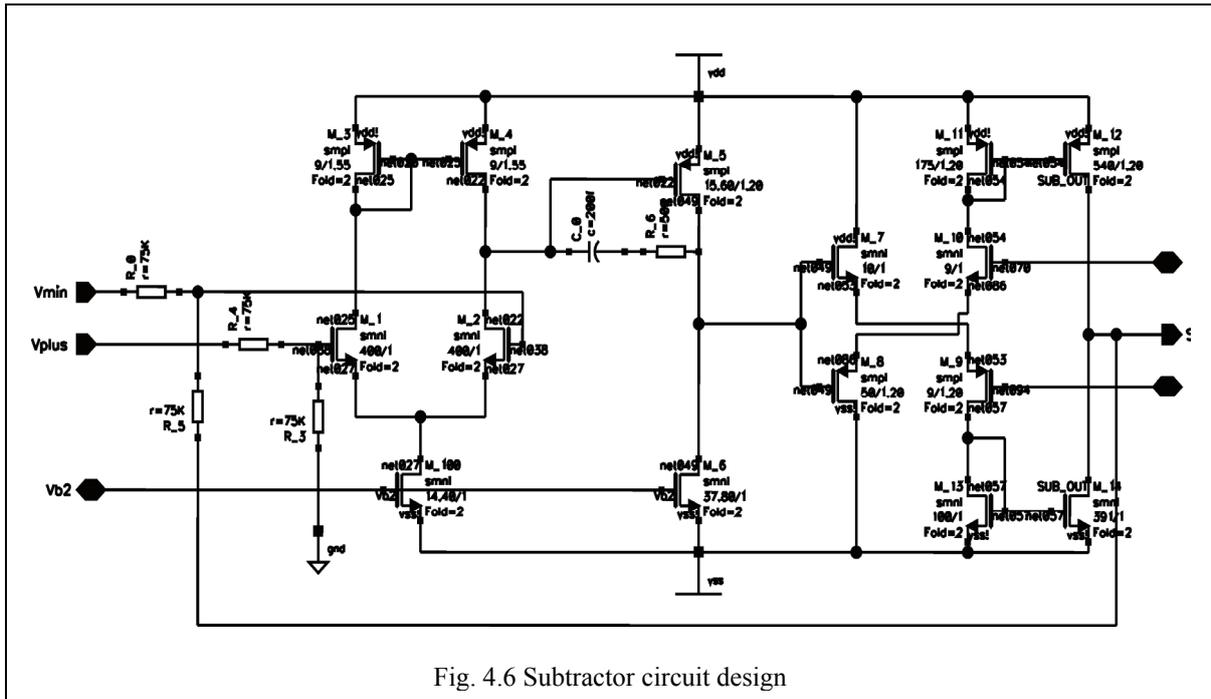
Fig. 4.6 Subtractor circuit design

A simulation of the subtractor is shown in figure (4.7). For the inputs a sinus at 500 Hz with 1 Volt and 0.996 Volt amplitude are used. The output of the subtractor is shown as *VN(OUT)*. The simulation also shows the calculated difference between the input signals, *Vdif*, which is added as a reference signal.

Simulation of the circuit shows a proper subtraction function. For very small differences (≥ 1 mV) the subtraction gets less accurate. The output becomes a little smaller which can be modelled as attenuation.
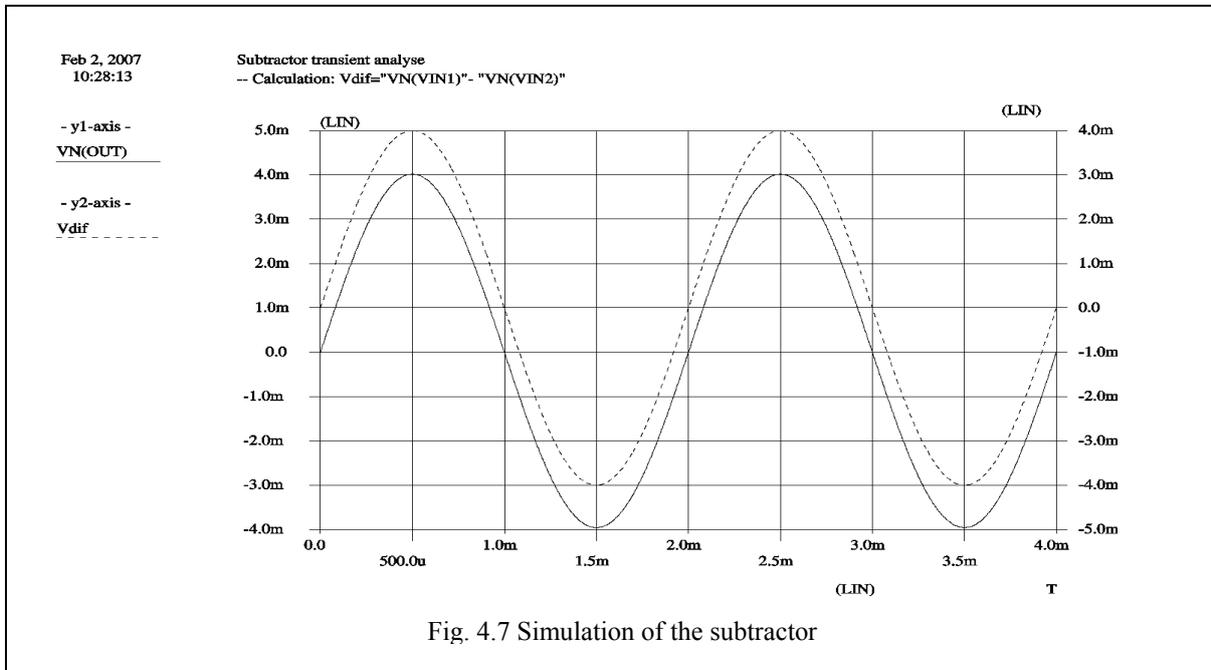

Fig. 4.7 Simulation of the subtractor

4.3 Loop Amplifier

The loop amplifier β is used to increase the loop gain of the piezo driver. It amplifies the error signal which is used to drive and/or correct the piezo driver output stage. In section 3.2.4 the gain of the amplifier was calculated at 308. To have some room for error the gain of the loop amplifier β is chosen smaller at 250.
The circuit realisation of the amplifier with the use of an op-amp can be seen in figure (4.8).
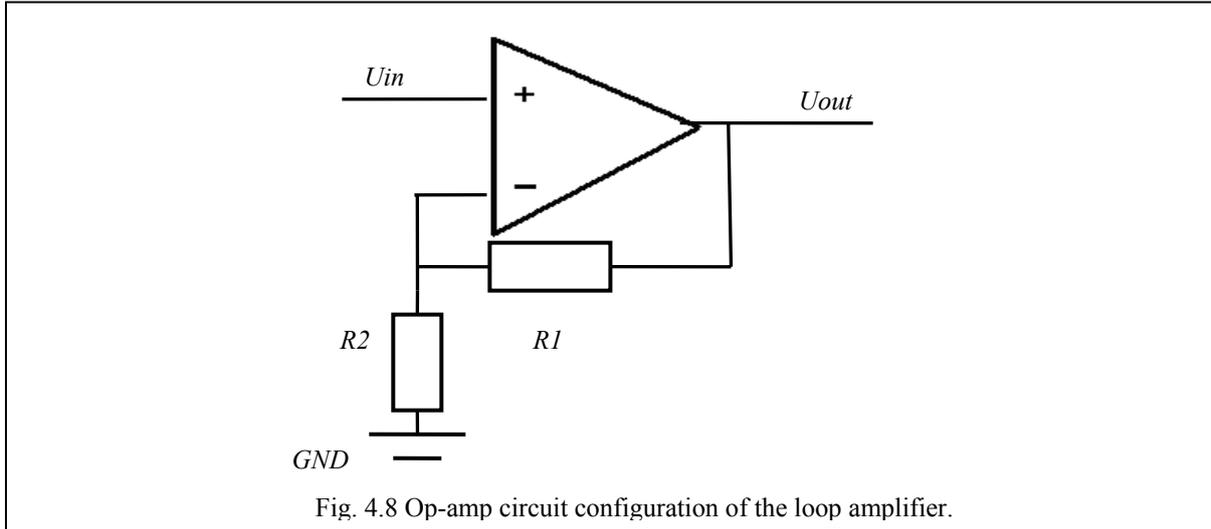

Fig. 4.8 Op-amp circuit configuration of the loop amplifier.

The gain of the op-amp circuit configuration can be calculated with equation (4.10).

$$G_{loop\,amp} = \frac{Uout}{Uin} = \left(1 + \frac{R1}{R2}\right) \quad\quad\quad (4.10)$$

To get a gain of 250 the ratio of the two resistors, R1 and R2, must be 249. To avoid influences of the output resistance of the op-amp resistor R1 is chosen large. Using formula (4.10) the resistance of both resistors should be 50 kΩ for R1 and 200 Ω for R2.

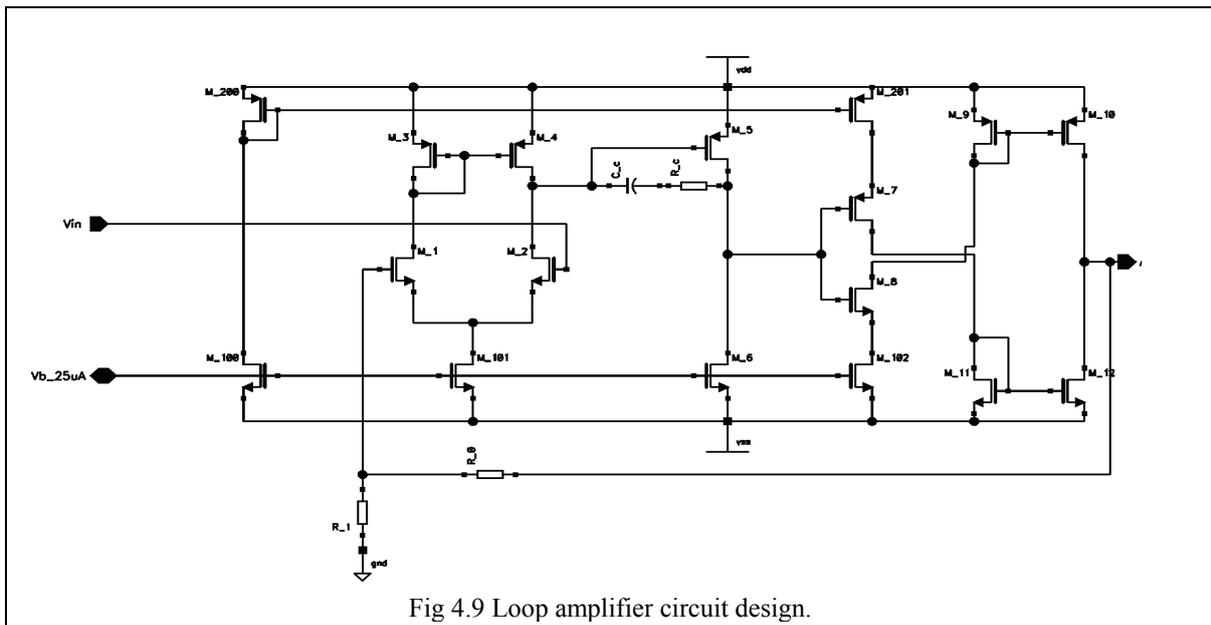Fig 4.9 Loop amplifier circuit design.

However, simulation shows that for a 250 gain the resistors *R1* and *R2* should be respectively 60 kΩ and 200 Ω. The output resistance of the op-amp does still influence the gain of the amplifier topology.

The simulation is illustrated in figure (4.10) and the circuit in figure (4.9). Appendix IX shows an enlarged version of the loop amplifier circuit design. The simulation shows clearly the 250 gain of the loop amplifier. The 4 mV input signal is amplified to a 1 Volt output signal.
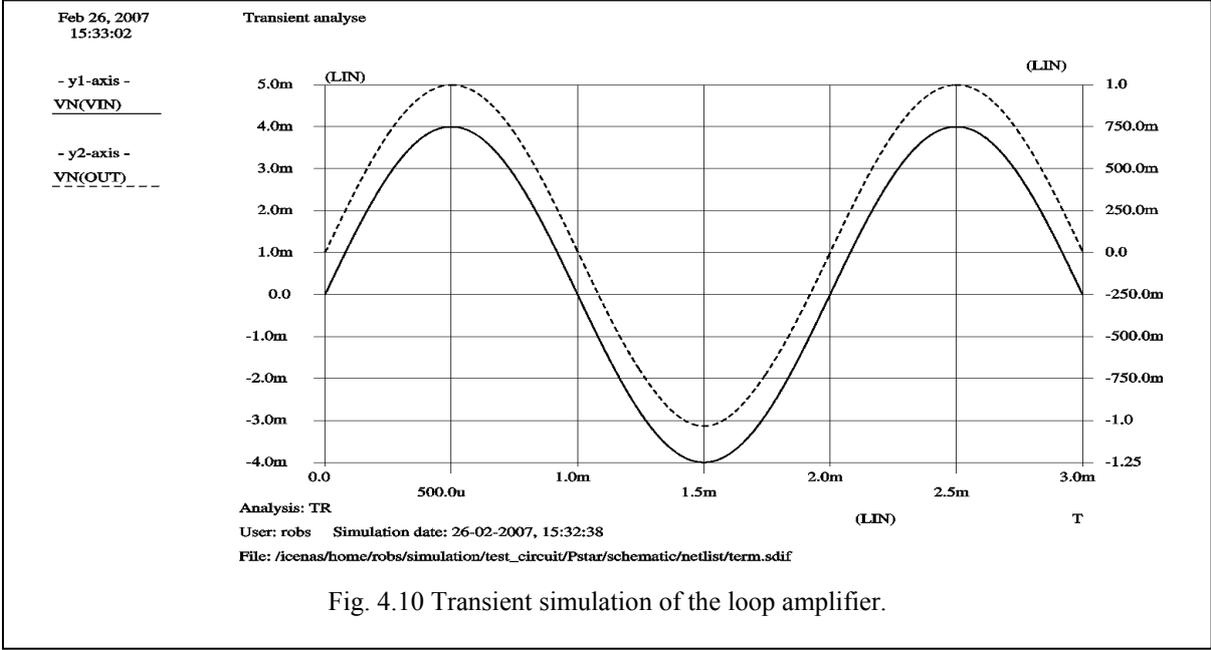

Fig. 4.10 Transient simulation of the loop amplifier.

4.4 Pulse Width Modulator

The pulse width modulator converts the input signal to a pulse width signal. It uses a reference signal, *Utriangle*, and comparator for the modulation of the signal. The reference signal is generated by a waveform generator in a separate circuit. The total PWM circuit design consists of the triangle generator and the comparator. The block schematic of the total PWM modulator is shown in figure (4.11).
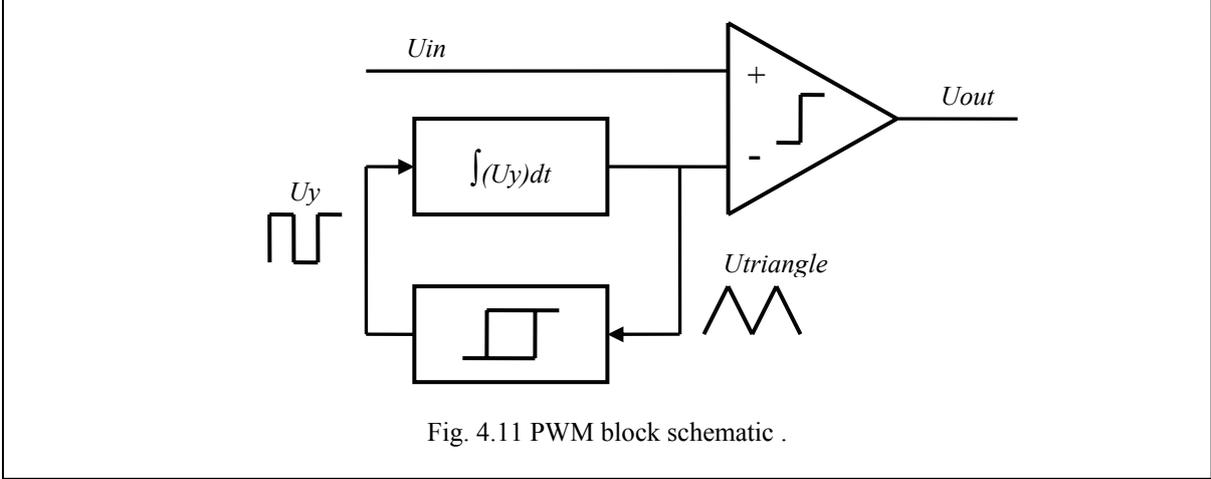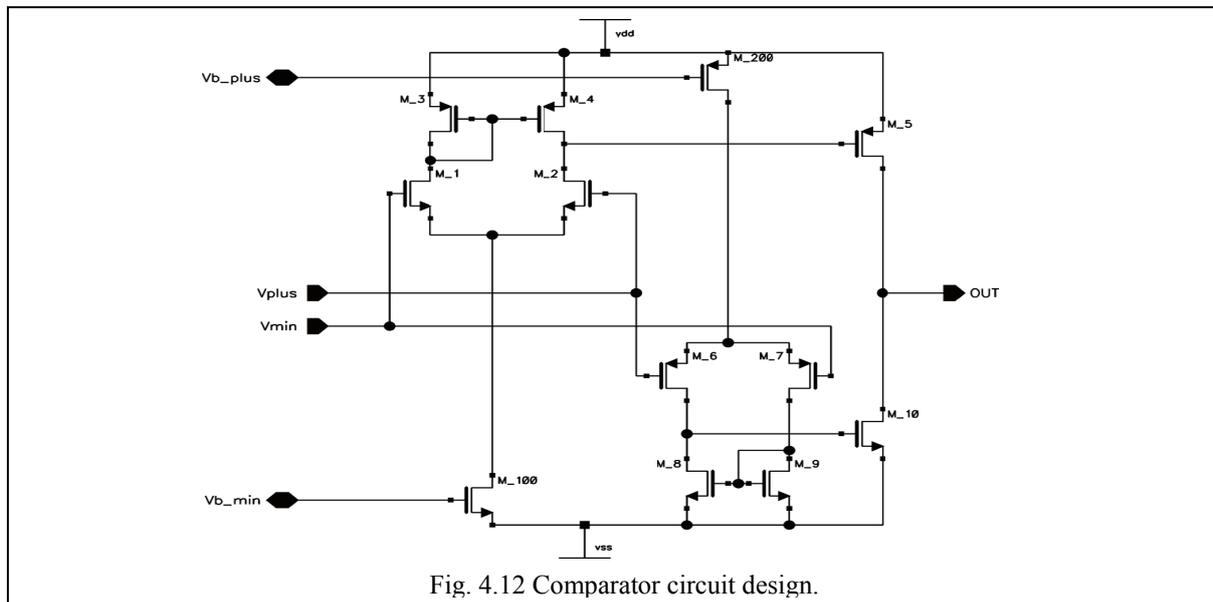

Fig. 4.11 PWM block schematic .

The basic function of the PWM is performed by the comparator. The design of the comparator circuit is similar to the two stage op-amp. It uses a two stage topology [25]. The comparator circuit can be seen in figure (4.12) and in appendix X.
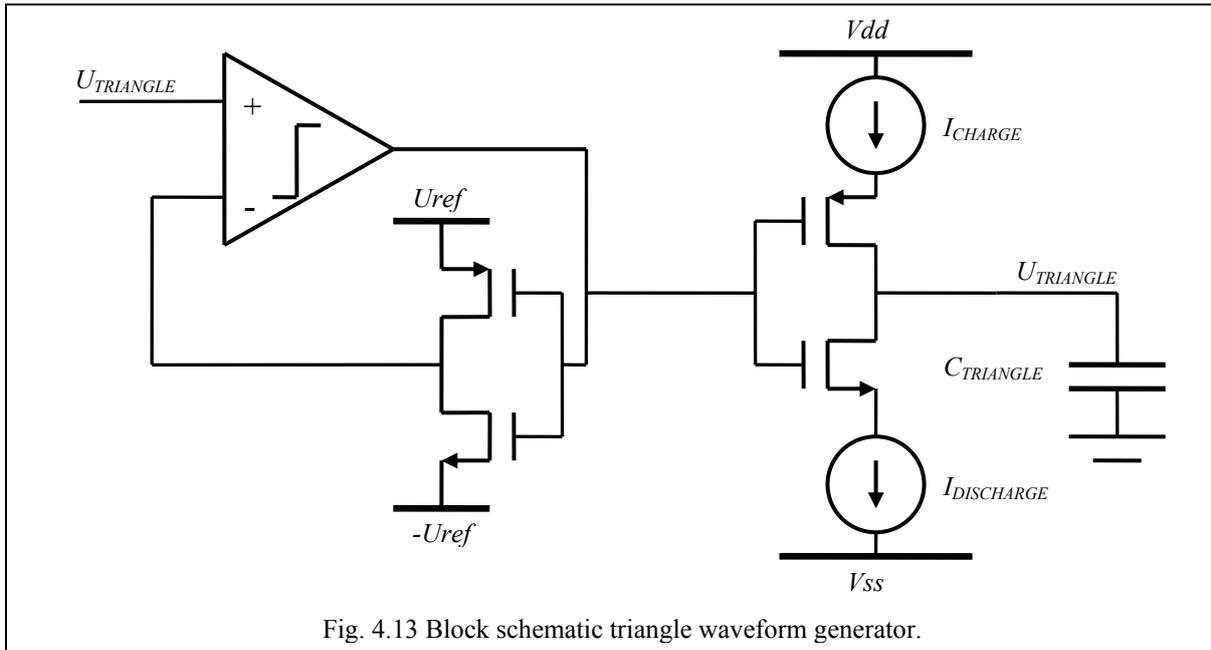

Fig. 4.12 Comparator circuit design.

The comparator is build with two OTA stages and an inverter output stage. One of the OTAs has a NMOS transistor input pair, *M1* and *M2*, which drives the PMOS transistor (*M5*) of the inverter output stage. The other OTA has a PMOS transistor input pair, *M6* and *M7* which drives the NMOS transistor (*M10*) of the inverter output. The OTAs are designed in such a way that a small difference between the two input voltages causes the output voltage to switch between high and low voltage.

The comparator works as follows. When the voltage at the V_plus input becomes higher than the voltage at the V_min input, the current through transistor *M2* becomes greater than the current through *M1*. The current of *M1* is mirrored by *M3* and *M4*. This causes the gate voltage of *M5* to drop. The other OTA performs a similar action causing the gate voltage at *M10* to drop. The PMOS transistor *M5* turns on and the NMOS transistor *M10* turns off. This causes the output to switch to the positive supply voltage.

The waveform generator has a conventional architecture consisting of an integrator and a Schmitt trigger in a positive feedback loop [26], see figure (4.11). The generator uses the output triangle waveform to switch between the two states of the triangle, positive and negative ramp. The switching between the two states is done by the Schmitt trigger. The switch level is determined by the reference voltage level of the Schmitt trigger. This automatically determines the amplitude of the triangle. The circuit can be realised with the use of a comparator and a switching reference voltage. The block schematic is displayed in figure (4.13).

The reference voltage, ±*Uref*, changes when the output of the comparator switches to the other state. An inverter transistor pair is used to switch between the two reference voltages. The comparator in the waveform generator controls the charging and discharging of the capacitor, $C_{TRIANGLE}$, as well. The capacitor functions as an integrator which creates the triangle waveform.

Fig. 4.13 Block schematic triangle waveform generator.

Charging the capacitor causes the positive ramp of the triangle. The capacitor is charged until the triangle voltage becomes greater than the reference voltage *Uref*. When this happens, the output of the generator's comparator switches to high. This causes the reference voltage to switch to *–Uref* and the capacitor to discharge. The capacitor is now discharged from approximately the positive reference voltage *Uref* to the negative reference voltage *–Uref*.

The amplitude of the triangle is determined by the reference voltage. The frequency of the triangle is determined by the charge current and capacitance of $C_{TRIANGLE}$. This can be calculated with the following equation (4.11).

$$2 \cdot \hat{U}_{TRIANGLE} = \frac{1}{2} \cdot \frac{1}{C_{TRIANGLE}} \cdot I_{CHARGE} \cdot T_{TRIANGLE} \qquad (4.11)$$

In one half of the period of the triangle is charged from *–Uref* to *Uref* and the second half of the period it is discharged. This is indicated by *2* and the *½* in the formula. In chapter three the amplitude of the reference voltage was chosen at 1 Volt. The frequency can now be determined by choosing appropriate values for the (dis)charge current and capacitor.

For a symmetric triangle waveform the charge and discharge current have to be equal. The (dis)charge current for $C_{TRIANGLE}$ needs to be constant and not be influenced by the switching of the surrounding circuits. A separate current mirror with feedback is applied to ensure a constant charge current [26]. The schematic can be seen in figure (4.14A). The current through R_{LOAD} gives a voltage which is used as feedback signal. The amplifier adjusts the voltage at the gate of the output transistor. In this way the voltage over the resistor is kept constant resulting in a constant load current.

The reference voltages for the Schmitt trigger design need to be constant as well. To ensure a constant voltage, a voltage buffer is used. The buffers use a bias voltage which is created in the power supply and is equal to the reference voltage. For now it is assumed that the power supply generates stable bias voltages. The block schematic of the voltage buffer can be seen in figure (4.14B).
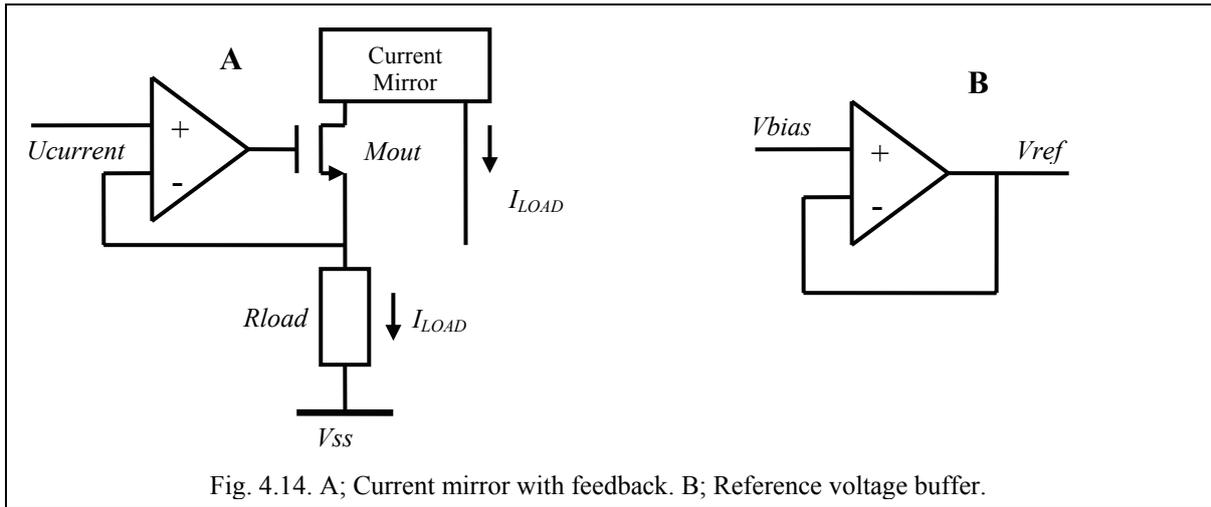
Fig. 4.14. A; Current mirror with feedback. B; Reference voltage buffer.

The two comparators in the total design for pulse width modulator use the same circuit configuration discussed earlier in this section. The complete design of the PWM can be seen in figure (4.16) or appendix XI. The comparator of the waveform generator is indicated as *Comparator* A and is formed by transistors *M1* to *M10*. The reference voltage buffer circuits and feedback of the current mirrors are realised with OTAs. These two circuits are indicated with *Voltage reference* and *Load capacitor* in figure (4.16). The PWM comparator is indicated with *Comparator B*.

The PWM has to be initialised at the start to ensure that the generator starts oscillating. This is done by initialising the reference voltage level and triangle voltage. The signals of the initialising are created outside the PWM. These have, for the time being, both been simulated with pulse sources.

The (dis)charge current is taken as 5 μA and the capacitor has been calculated with a capacitance of 1.25 pF. This gives a frequency of 1 MHz which can be seen in the simulation showed in figure (4.15).
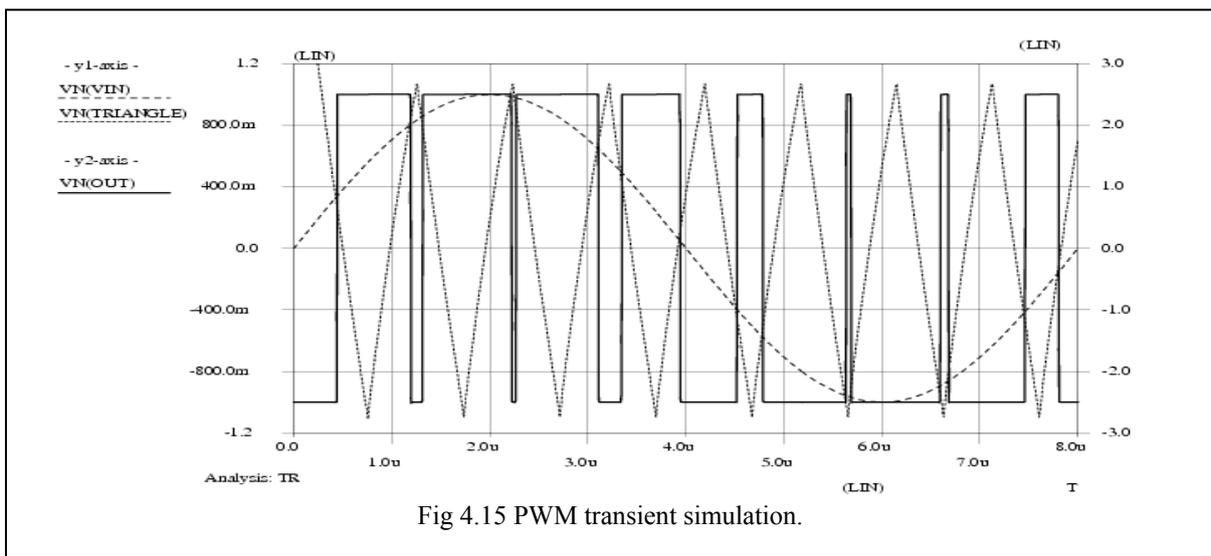

Fig 4.15 PWM transient simulation.

The triangle has slightly bigger amplitude than the reference voltage of 1 Volt. This caused by the switching delay in the circuit. The simulation shows clearly the pulse width modulation of the PWM.
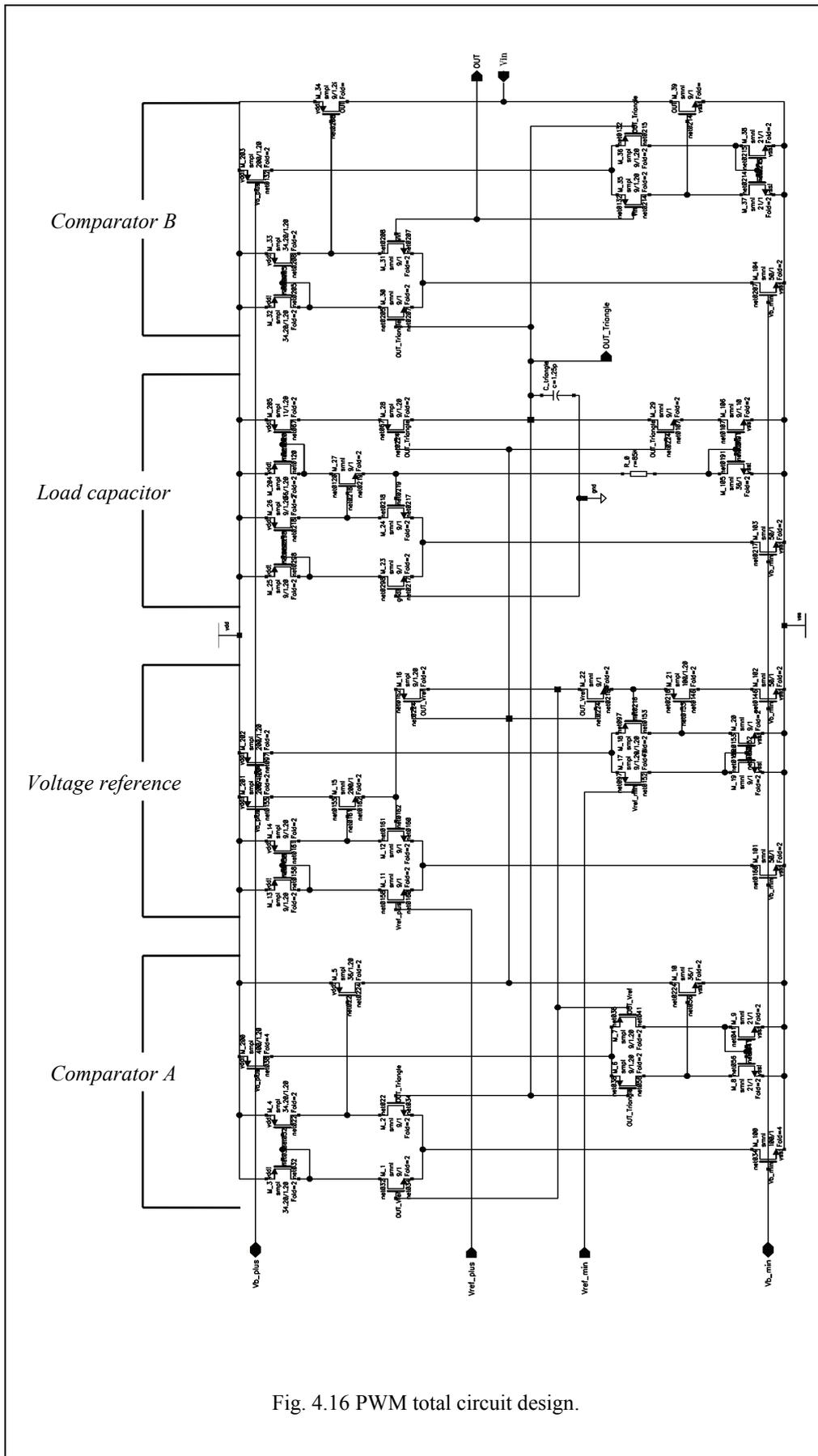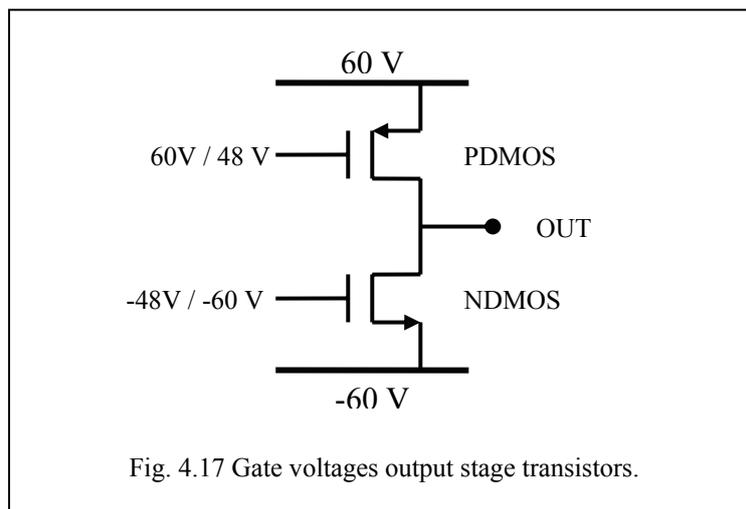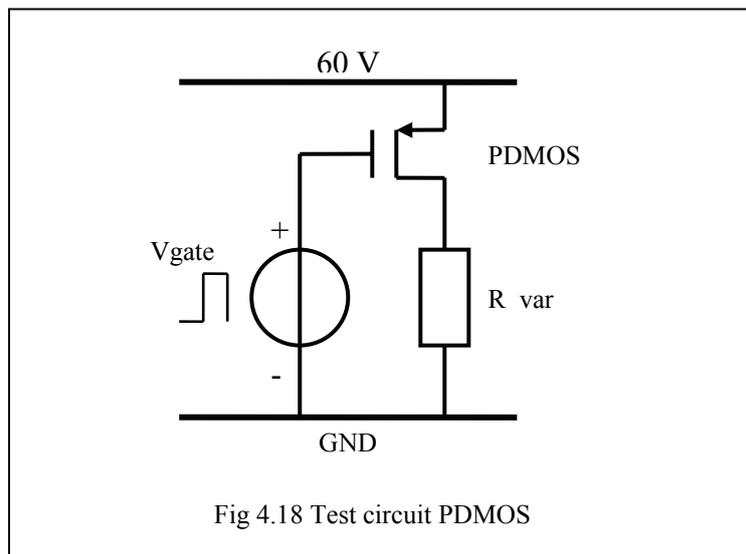
Fig. 4.16 PWM total circuit design.

4.5 Output Stage

The output stage is used to switch between the positive and negative power supply to form the high voltage output pulses. An ehv_NDMOS and ehv_PDMOS are used for this task. The extra high voltage DMOS transistors are needed because the maximum voltage drop over the transistors can be twice the supply voltage. This gives a drain-source voltage of 120 Volt. The ehv_DMOS transistors need a gate-source voltage of 12 V and 0 V to switch off and fully on. The needed gate voltages are indicated in figure (4.17).

Fig. 4.17 Gate voltages output stage transistors.

The dissipation in the transistors, as indicated in chapter three, depends on the size of the output transistors. To find the optimal size several simulation where done with different widths for the NDMOS and PDMOS. The transistors are tested separately from each other. The test circuit of the PDMOS is shown in figure (4.18), the NDMOS uses a similar circuit.

Fig 4.18 Test circuit PDMOS

The dissipation of the transistor is determined by measuring the power delivered by the 60 Volt supply source and the gate source. The power dissipated in the resistor, *R_var*, is of course not taken along in the dissipation of the transistor.
The dissipation is calculated over one complete switching cycle with a frequency of 1 MHz. The conduction losses are simulated with the use of the variable resistor *R_var*. This resistor

has a variable resistance which keeps the current through the transistor constant at the RMS value of the maximum output current. In chapter one the maximum current was calculated at 94 mA, equation (1.2).

The switching, transition and conduction losses have been measured with this circuit for varies widths of the output transistors. The results can be found in figure (4.19) for both transistors.
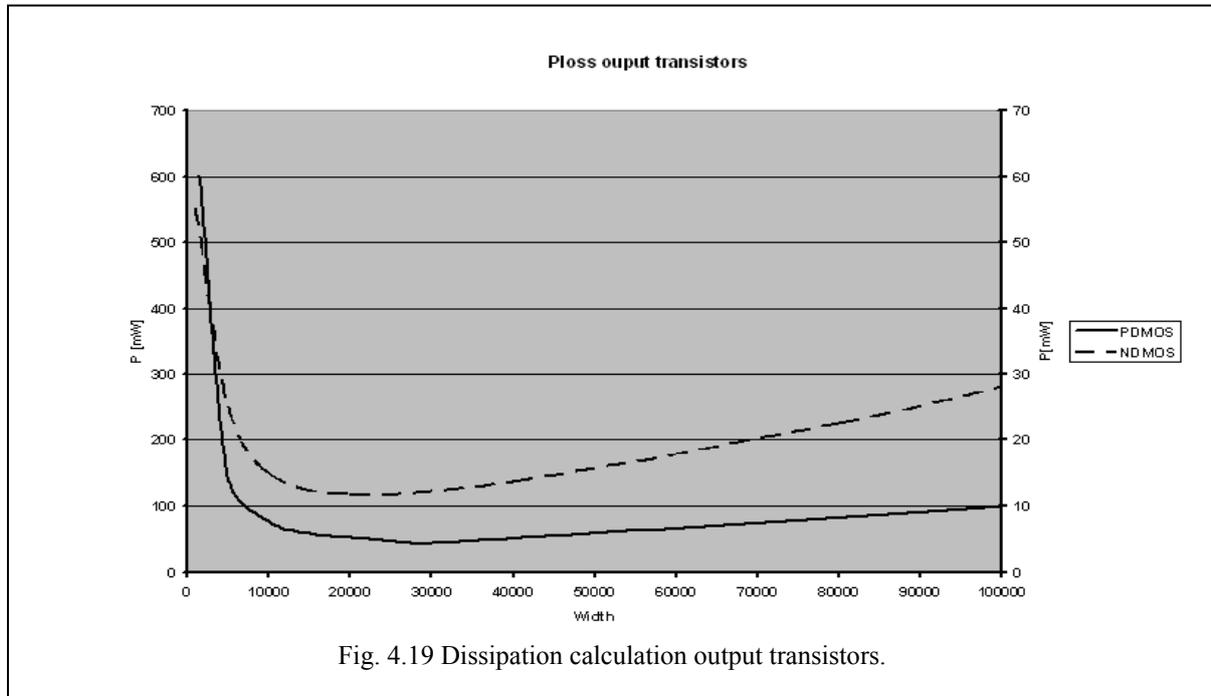

Fig. 4.19 Dissipation calculation output transistors.

The best size for widths for the PDMOS and NDMOS are respectively 30000 and 15000. These values will give the least dissipation and will therefore be used for the output stage transistors.

The two output transistors need high gate voltages to switch on and off, see figure (4.17). The PWM is not capable of producing these high voltages to drive the two output transistors. This has to be done with another circuit, called the gate driver. This block transforms the pulse signal of the PWM to the correct gate voltage for the two output transistors.

Furthermore the gate driver controls the turn-on timing of the output transistors. Output transistor turn-on timing prevents the output transistors to conduct at the same moment. The output stage transistors have very low on resistance. It is therefore important to avoid situations in which both transistors are on simultaneously, as this would create a low-resistance path from VDD to VSS through the transistors and a large shoot-through current.

At best, the transistors will heat up and waste power; at worst, the transistors may be damaged. Break-before-make control of the transistors prevents the shoot-through condition by forcing both transistors off before turning one on. The time interval in which both transistors are off is called dead time.

The gate driver system has several sub-functions to fulfil its tasks. The different functions are illustrated in figure (4.20) and appendix XII. The gate driver contains three different functions, a logic function (*gate logic*), level shifter (*level shifter and gate observer*) and driver (*pdriver and ndriver*). These blocks will be discussed in the following sections.
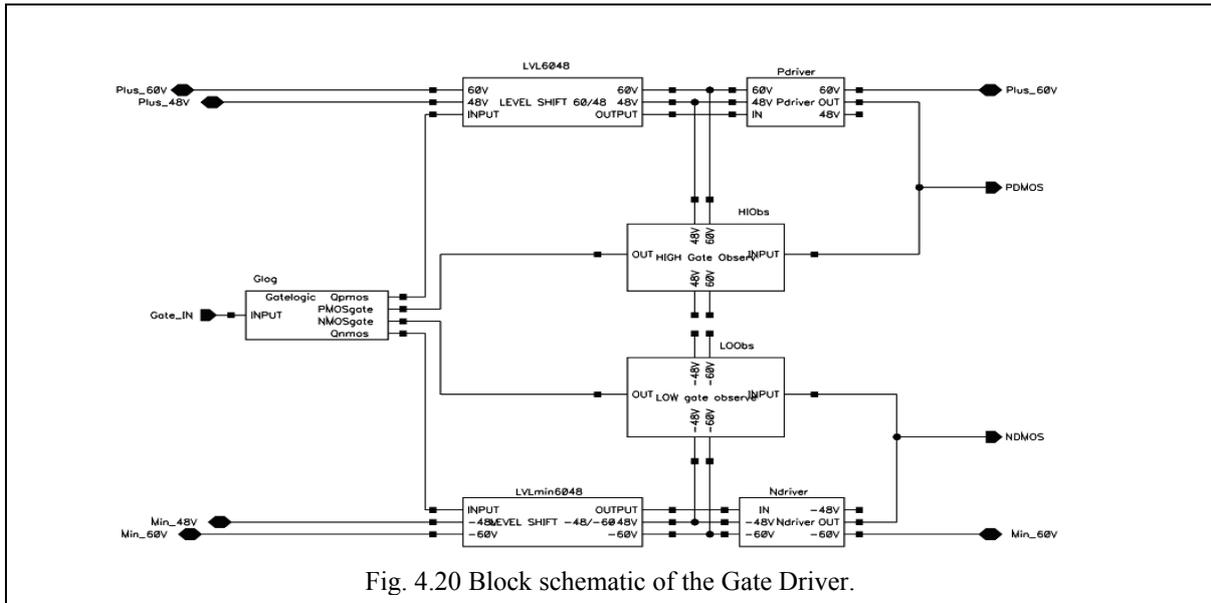
Fig. 4.20 Block schematic of the Gate Driver.

4.5.1 Gate Logic

The pulse signal of the PWM is inserted into the gate logic block. This block controls the on and off switching pulses off the two output transistors and with that prevents the output transistors from conducting at the same moment. It uses the PWM signal and the gate voltage of both output transistors to determine the correct driving signals for them. The performed function of the gate logic is also referred as handshake protocol **[27]**. The logic function is determined with table (4.1).

Input	NMOS gate	PMOS Q
L	L	H
L	H	H
H	L	L
H	H	H

Input	PMOS gate	NMOS Q
L	L	L
L	H	H
H	L	L
H	H	L

Table 4.1 Logic function gate driver.

The left table is used to find the states to switch the PMOST and the right table is used to find the switching states for the NMOST. The input column gives the state of the input signal, *L* indicating low voltage and *H* high voltage.
The two columns of *NMOS gate* and *PMOS gate* show the voltage level on the gate of the two transistors. The signals which the gate logic has to generate for the driving of the NMOS and PMOS are shown in the *PMOS Q* and *NMOS Q* columns.
The logic equations for the signal of the NMOS and PMOS are given in (4.12) and (4.13).

$$Q_{PMOS} = \overline{Input} + NMOS_{GATE} \tag{4.12}$$

$$Q_{NMOS} = \overline{Input} \cdot PMOS_{GATE} \tag{4.13}$$

The logic equations can be realised as shown in figure (4.21). It uses an inverter for the input and an *OR-port* and an *AND-port* for respectively the *Qpmos* and *Qnmos* signal.

Fig 4.21 Block schematic gate logic.

The block schematic of the gate logic is transformed to a transistor design. This circuit design is illustrated in figure (4.22) and appendix XIII

Fig. 4.22 Gate logic circuit design .

The gate logic uses the low voltage supply sources of 2.5 V and -2.5 V. The *OR-port* and *AND-port* are realised with respectively a *NAND-* and *NOR-port* which are inverted at the output. Both outputs, Q_{PMOS} and Q_{NMOS}, are buffered with two inverter pairs. The $PMOS_{GATE}$ and $NMOS_{GATE}$ inputs are both buffered with a Schmitt trigger to filter out the switch spikes. It further transforms a signal with a slow or sloppy transition into a signal with a sharp transition [28].

The CMOS Schmitt trigger circuit and transient analyse are showed in figure (4.23). The transfer characteristic has the shape of a hysteresis curve, due to the regenerative effect of the transistors *M4* and *M7*, for high threshold and *M5*, for low threshold. Transistor *M3* turns on when *Vin* is lower than:

$$Vin \leq Vth_P + V_Y \tag{4.14}$$

Fig. 4.23 CMOS Schmitt trigger circuit and transient analyse.

The node voltage *Vy* is determined by transistors *M0* and *M5*. When *Vin* is low enough transistor *M0* starts to conduct causing a higher voltage on node *Vy*. When the input voltage reaches the Schmitt triggers low threshold level, the gate-source voltage of *M3* is low enough to start conducting. This switches the output to *Vdd*.
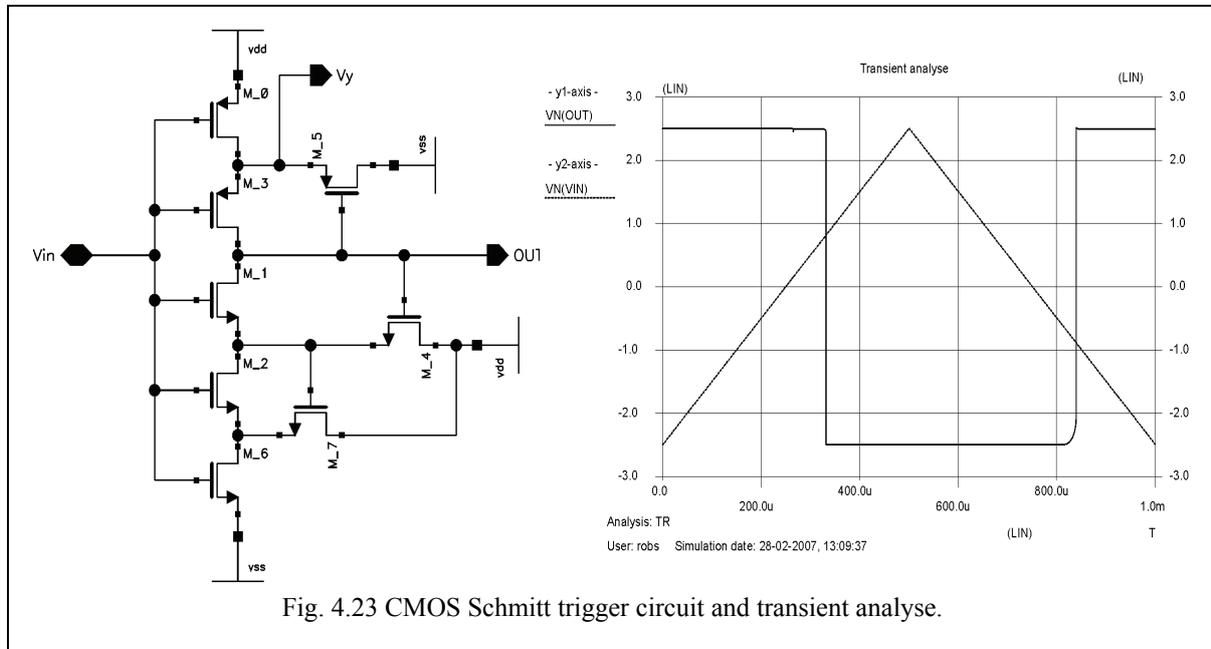
The NMOS-branch uses two stages for the high threshold. This is because the NMOS transistors have a lower Vth_N causing a lower threshold value for one stage. Using two stages increases the threshold voltage. The threshold voltages are 0.8 Volt and -0.8 Volt.

To compensate the inverter action of the Schmitt trigger an extra inverter stage is placed after it.

4.5.2 Level shifter

The level shifter is needed to transform the gate logic output signal the correct voltage levels to drive the output stage transistors. The PDMOS output stage transistor requires 48V and 60V at the gate to switch on and off. The NDMOS requires a similar voltage shift of -48V and -60V. The gate logic uses the gate voltages of the two output stage transistors. These voltages have to be shifted down to the low voltage supplies for the gate logic. The circuit design of the four level shifters is similar. Therefore only the level shifter from -2.5V and 2.5V to 48V and 60V will be discussed.

The circuit design is given in figure (4.24) and in appendix XIV. The input and output of the level shifter are each buffered with two inverters stages which are respectively *M20 − M23*

and *M10 – M13*. The level shifter works with two inverter pairs at high voltage (*M0 M1* and *M2 M3*) and four pull down transistors (*M4 – M7*) between the high and low voltage.
The inverter pairs at the high voltage have their gates connected to the output of the other inverter stage. This causes inverter *M0 M1* to switch when the output of inverter *M2 M3* is changed and vice versa.
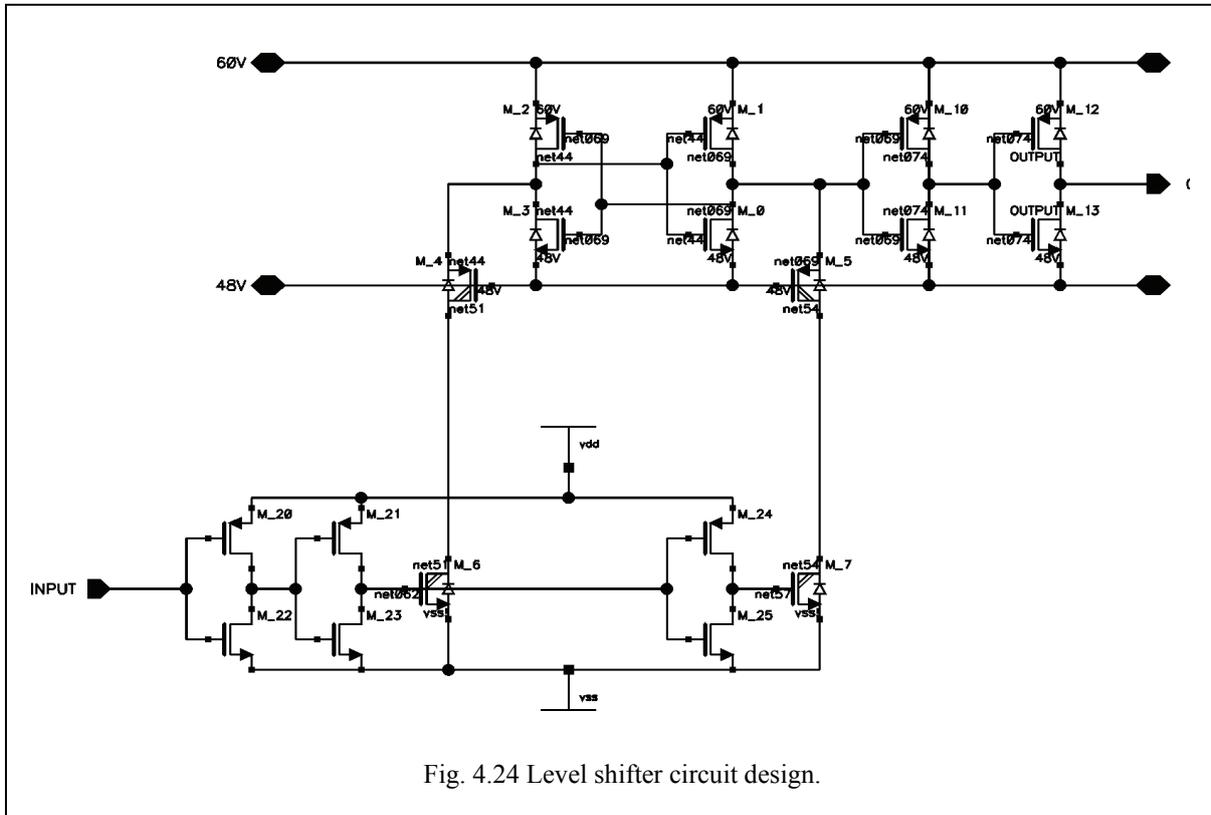

Fig. 4.24 Level shifter circuit design.

The inverter pairs at the high voltage side are realised with lv_DMOS tranisitors. Those are required because of the 12 Volt difference between the high supply voltage lines, see figure (4.24). For the pull down transistors hv_DMOS are used. These operate between the high supply voltage (60 V) and low supply voltage *VSS*, causing a large voltage difference. The inverter pairs at the low side are realised with normal PMOS and NMOS.

Now when the level shifters input changes from low to high, the pull down transistor *M6* is turned on. Current is drawn from the inverter pair *M2 M3* via *M4* to *Vss*. This causes the voltage on the output of the inverter to decrease. When the source voltage of *M4* becomes to low it turns *M4* off. The pull down transistors *M5* and *M7* are used in a similar way to let the level shifter output switch from high to low.
If the current drawn out of the high inverter pair is large enough then the two high inverter pairs will switch states. The output of the level shifter is switched from low to high (48V to 60V). For a proper function of the level shifter the pull down transistors have to be large in order draw more current out of the high inverter pairs then the transistors in the high inverter pair can deliver.

A transient simulation of the level shifter is shown in figure (4.25). The switching of the level shifter takes some time. This introduces a small delay between the input and output.

Fig. 4.25 Level Shifter transient analyse.

4.5.3 Driver

The two output stage transistors are quite large and because of that have large gate capacitance. In order to switch the output stage transistors on and off fast enough a driver is needed. The driver consists of several inverter stages with increasing transistor size. The number of inverter stages needs of course to be an even number. For the switching of the PDMOS and NDMOS output stage transistor, four and two inverter stages are used respectively. In figure (4.26) the driver for the PMOS transistor is shown.

Fig. 4.26 Driver circuit design.

The last inverter pair has to be designed with care because this pair determines the on and off switching time of the output stage transistor. Another important design issue is that the output stage transistor must stay off when needed, especially when the other output stage transistor is switched on.

In figure (4.27) the two output stage transistors are shown together with the last inverter pairs of both drivers.

When the PDMOS is off, the gate is kept high by *M1*. Now the NDMOS is switched on creating a path to negative supply source. This affects the gate-drain capacitance of the PDMOS, *Cgd_p*. Charge is removed out of the capacitor causing the gate voltage of the PDMOS to drop. If transistor *M1* is large enough the charge removal can be compensated, if not the gate voltage will drop below the threshold of the PDMOS causing it to switch on. This has to be avoided because large currents can flow directly from the positive to the negative supply voltage.
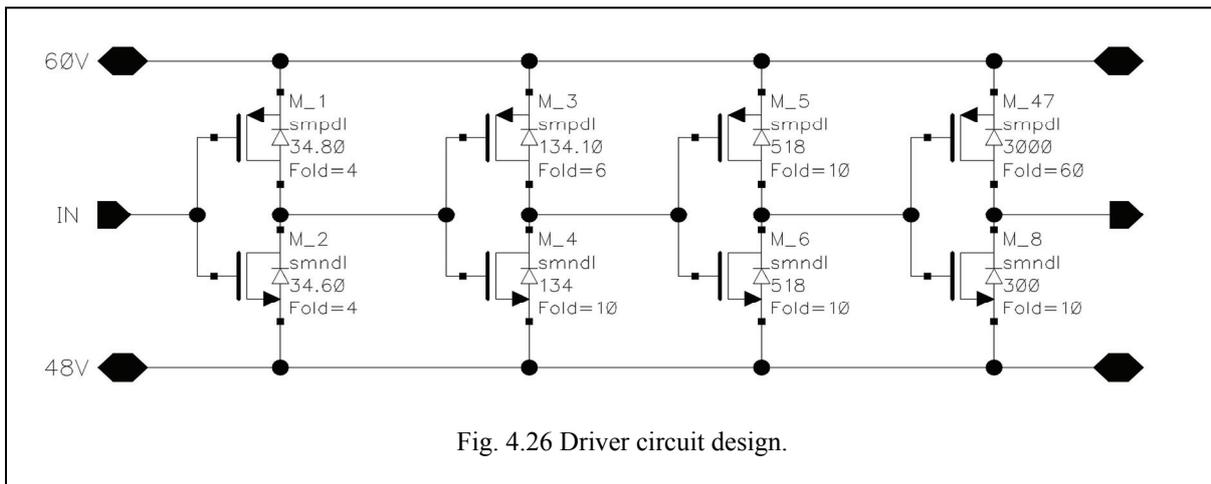
The transistor *M1* should be taken large enough to compensate for the charge removal. The size is determined by the size of the NDMOS and on the size of *M3* which determines how fast the NDMOS is

Fig 4.27 Switching on of the output stage transistor.

switched on. A similar approach can be made for the size of transistor *M4* which is used to switch the NDMOS off and keep it off. So both drivers for the NDMOS and PDMOS should be adapted to each other. First *M2* and *M3* are determined for a satisfying turn-on speed and the transistors *M1* and *M4* are adapted to this.

4.5.4 Total output stage

The simulation of the level shifter (fig. 4.25) showed some delay. All the sub-functions of the output stage together will cause a certain delay. The simulation of the input and output is shown in figure (4.28)
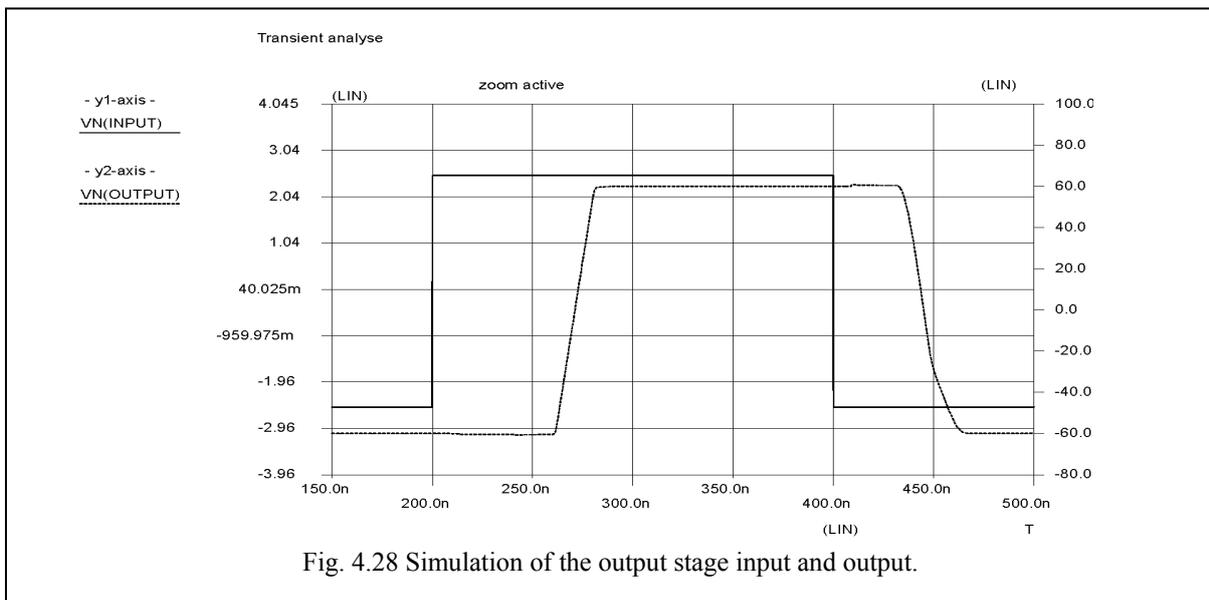

Fig. 4.28 Simulation of the output stage input and output.

As can be seen in the simulation of the output stage, the switching from low-to-high has a delay of 80 ns. For the high-to-low switch a delay of approximately 60 ns is simulated. The simulation also shows the time needed for the two output transistors to switch fully on. For both transistors this is approximately 20 ns.

4.6 Total circuit design of the Piezo Driver

All the necessary functions for the piezo driver have been designed. The total piezo driver system will look like figure (4.29), see also appendix XV.

Fig. 4.29 Total circuit design piezo driver.

The design starts with the two input buffer, to buffer the input and feedback signal (*Vsense*). The two buffers are connected to the subtractor which provides the error signal. The error signal is 250 times amplified by the amplifier. Next the signal is pulse width modulated and supplied to the gate driver. The two output transistors *M0* and *M1* are connected to the filter.

Before the system can be simulated some final adjustments have to be made. The sub-functions in the system as well as the output filter cause a shift in the phase, see figure (4.30A). In chapter three the phase characteristic of the filter was discussed. The filter shows a shift of almost 180° at the resonance frequency and after this the phase shift turns gradually back to 90°. Together with the phase shift of the circuits, the total phase shift could result into instability of the system. The phase shift of the sub-functions has to be tuned to avoid instability.

The circuits which use an op-amp configuration can be adjusted with the compensation capacitor and resistor as discussed in section 4.1. The phase shift has to be kept zero until after the resonance frequency of the filter.
In figure (4.30A) the phase characteristics of the circuit and filter are shown. The phase shift caused by the piezo driver sub-functions input buffer, subtractor and loop amplifier is indicated with the solid line. The input is applied to the buffer and the output is taken from the loop amplifier output. The PWM modulator and output stage are left out of the AC simulation because these cannot be simulated in an AC analyse.
The dashed curve represents the phase shift caused by the output filter. This transfer function uses the input of the filter and the feedback signal (*Vsense*) as the output signal. The sub-functions part and output filter are simulated separately in the graph of figure (4.30A). Adding

the two phase graphs of figure (4.30A) will give the total phase shift of the complete piezo driver. The phase shift of the complete piezo driver design is also simulated in figure (4.30B).

The phase shift of the total piezo driver has to be kept as small as possible until the open-loop transfer function (input signal to the feedback signal, *Vsense / Vin*) of piezo driver reaches 0 dB, see figure (4.30B). By tuning the circuits the phase shift is 151° at 0dB.

Fig 4.30 Transfer functions A; Phase shift of the Piezo Driver circuits and phase shift of the output filter, B; Open-loop Piezo Driver.

5. Simulation

The total circuit design of the piezo driver will be tested in this chapter. The functionality of the piezo driver will be examined with the use *Pstar*. Further the circuit will be checked on satisfying the requirements. The requirements where discussed in chapter one. A short summary of these can be found in table (5.1).

System electric requirements	System physical demands
• Output amplitude 60 Volt • Gain of 60 • Bandwidth 20-500 Hz • Max. phase shift 5° • Max. THD 3% • Stable for given piezo-patch range • Low dissipation • Adapted to behaviour piezo-panel	• Max. thickness 10 mm • Piezo driver system on piezo-panel • Number of components as small as possible

Table 5.1 system requirements

The programs used for the simulations are *Cadence* and *Pstar*. The simulation will be preformed (partly) on the piezo driver circuit design showed in figure (4.27) and appendix XV. The piezo is modelled with the equivalent circuit model discussed in section 2.3. The used component values are listed in table (5.2).

			Res. 1	Res. 2	Res. 3
C_p	125 nF	C_{res}	75 nF	15 nF	8 nF
R_s	25 Ω	L_{res}	1 mH	375 μH	316.5 μH
R_p	8 MΩ	R_{res}	35 Ω	45 Ω	65 Ω

Table 5.2 Piezo panel equivalent circuit component values.

Simulation of the total circuit does however take quite some time, about two days. To do all the simulations would take a lot of time which is, because of the little time left in the project, a problem.

The simulation time is reduced by replacing the output stage (gate driver and output transistors) with a controlled voltage source for some of the simulations. The output stage and the controlled voltage source are simulated to show the functionality of both circuit implementations. The first simulation uses the circuit shown in figure (5.1). The PWM circuit, gate driver with output transistors and the filter are used in this simulation.

Fig. 5.1 PWM and output stage simulation circuit.

The PWM and output filter are used in the simulation to show that the output stage works correctly with the PWM and filter connected to the output stage. The "PWM-output stage" simulation can be seen in figure (5.2).
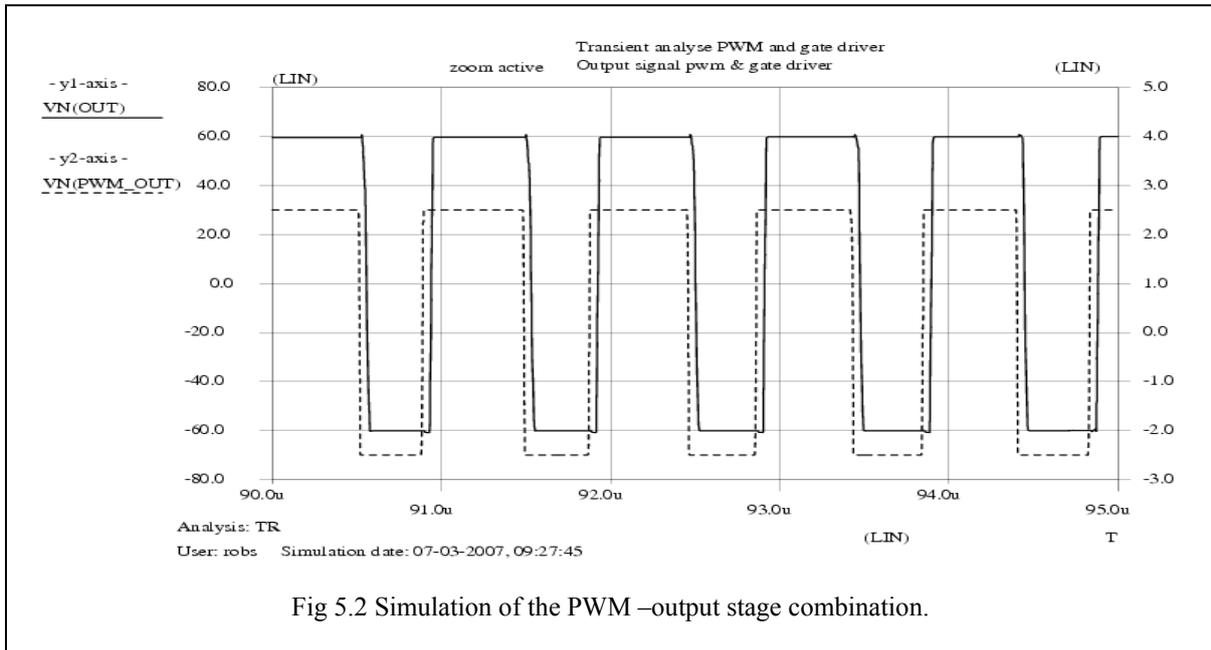

Fig 5.2 Simulation of the PWM –output stage combination.

The simulation shows the output of the PWM, *VN(PWM_OUT)*, and the output signal of the output stage (*VN(OUT)*). The output stage amplifies the pulses to plus and minus 60 Volt with a delay of approximately 80 ns.

For the next simulation the output stage is replaced by the controlled voltage source. This voltage source amplifies the output pulses of the PWM to plus and minus 60 Volt with a delay equal to the maximum delay of the gate driver (80 ns). The circuit used for the simulation is showed in figure (5.3).
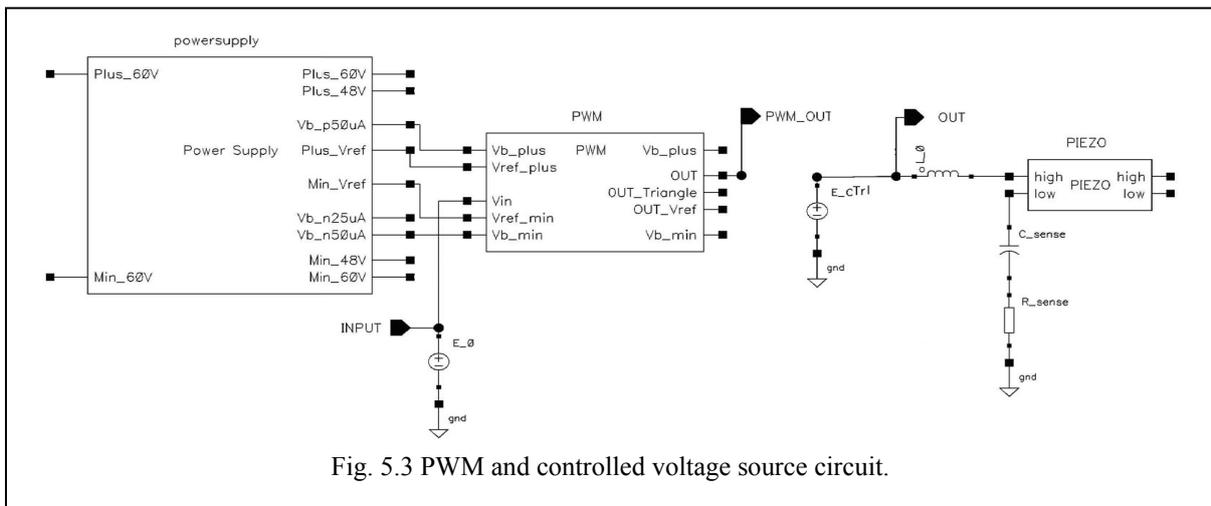

Fig. 5.3 PWM and controlled voltage source circuit.

The simulation of the "PWM-Controlled Voltage Source" is showed in figure (5.4). The intention is to show that this simplified circuit gives a similar output signal as the "PWM-output stage" combination. The output of the PWM is shown and the output of the controlled voltage source (*VN(OUT)*).
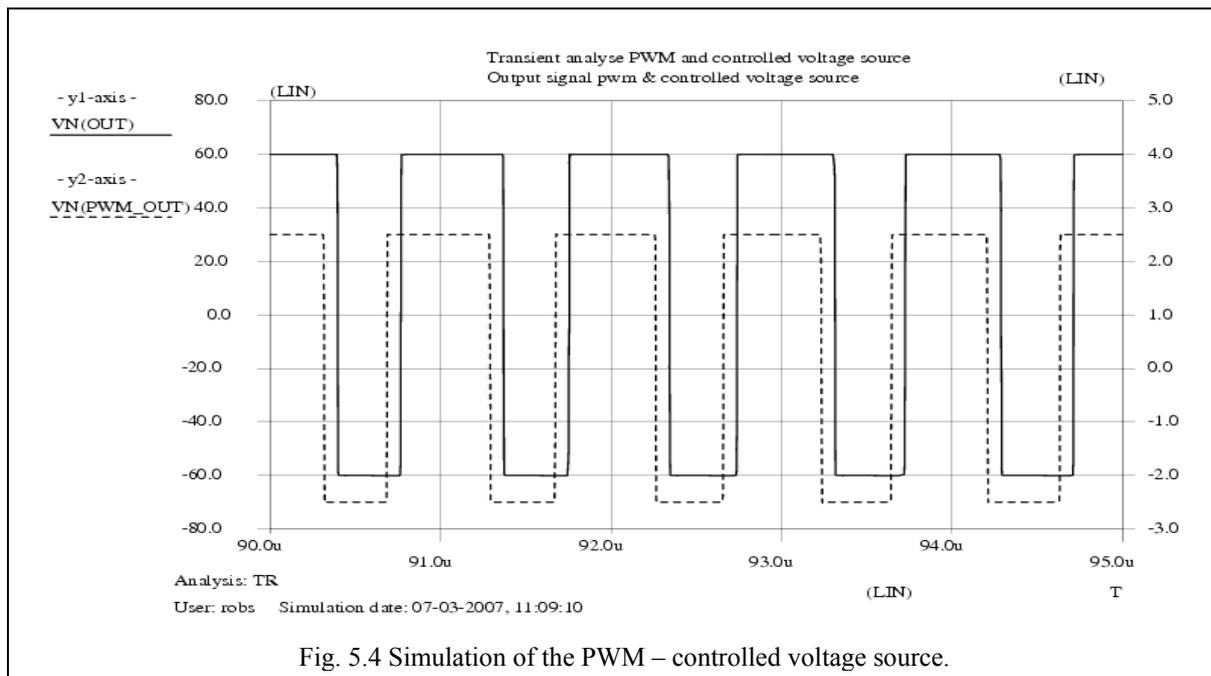
84

Fig. 5.4 Simulation of the PWM – controlled voltage source.

When comparing the two simulations of figure (5.2) and (5.4), it can be seen that the two graphs are very similar. The output pulses of the output stage (fig. 5.2) have a less steep slope than the output pulses of the voltage controlled source (fig. 5.4). It is assumed that the use of a controlled voltage source will cause no difference in the outcome of the simulations and can there fore be used in the piezo driver design and reduce the simulation time.
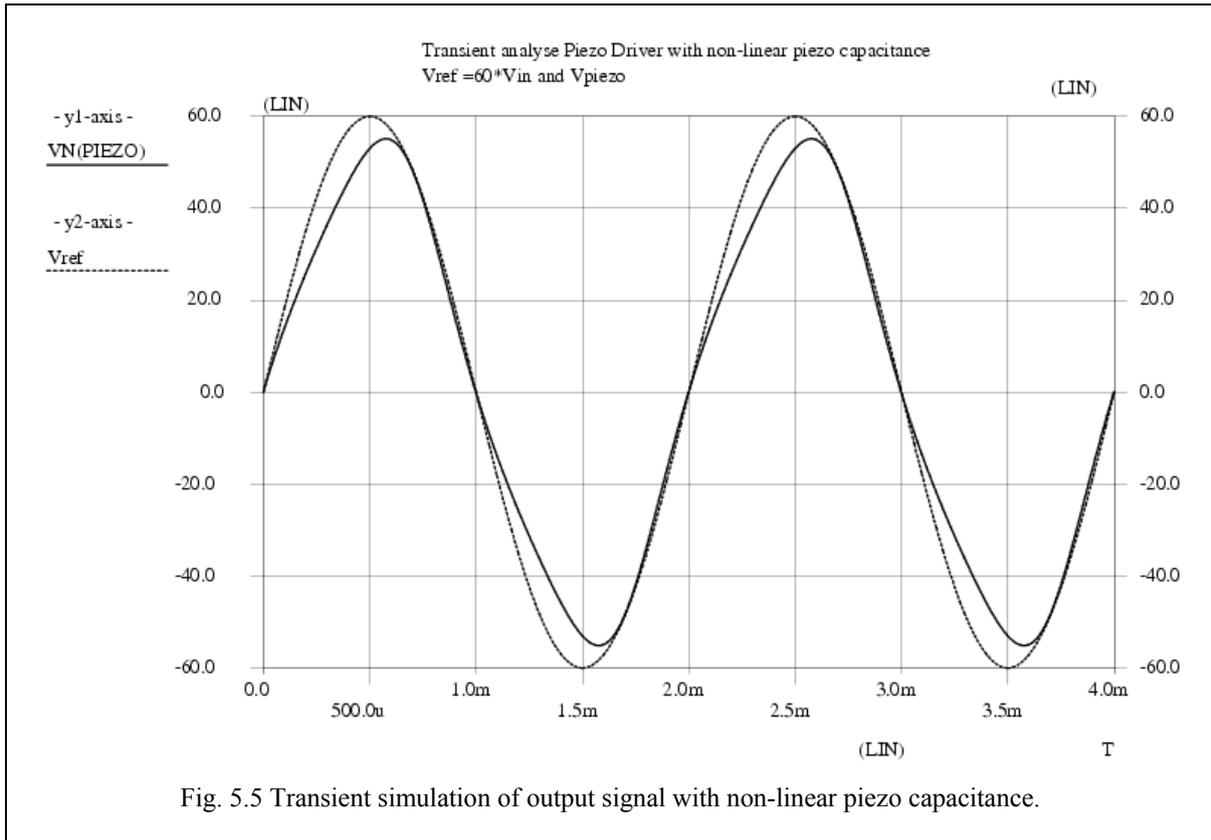
5.1 Transient analyse

All the tests which are done with a transient analyse of the piezo driver system will be discussed in this section. The input signal which is used for the transient simulation is:
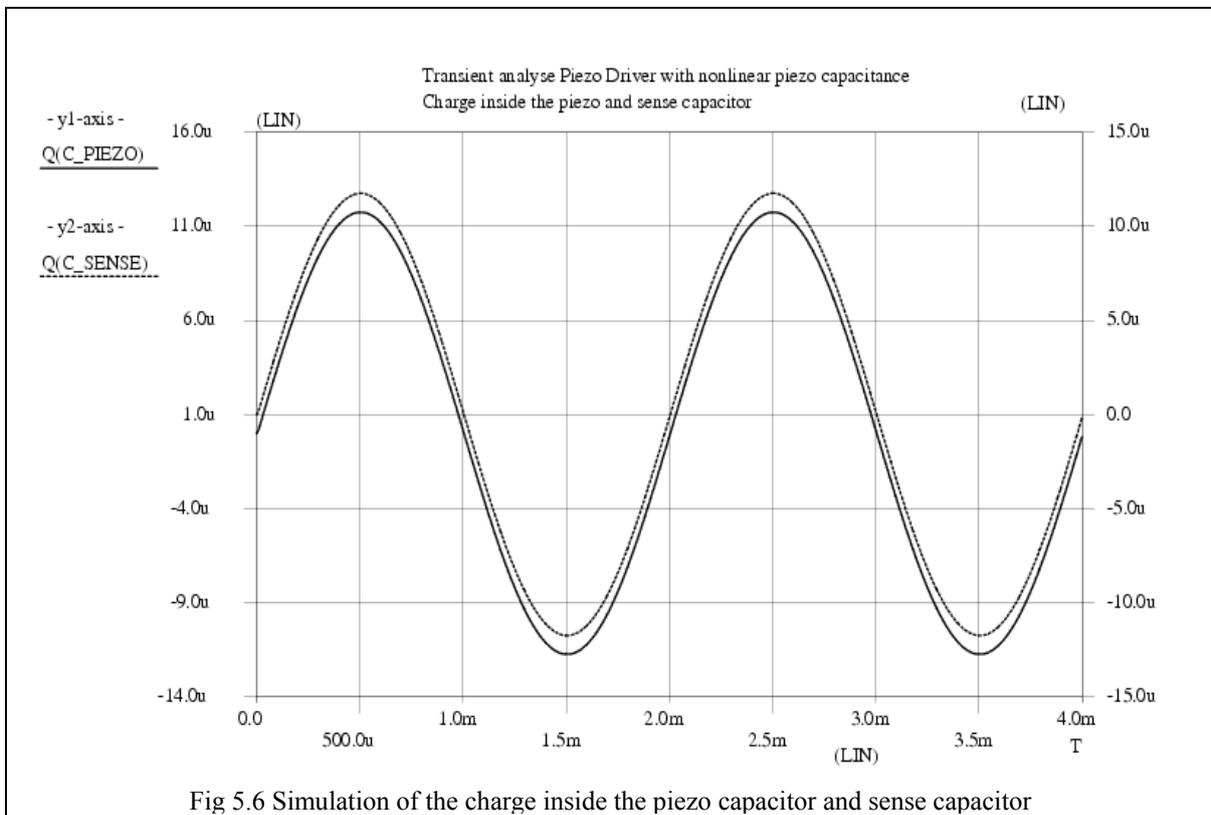
- Sinusoidal
- 1 Volt amplitude
- 500 Hz

The piezo driver is designed with charge control feedback to cope with the non-linear behaviour (hysteresis) of the piezo element. To test the charge control of the system a non-linear capacitor is used as the piezo capacitor. Figure (5.5) shows the transient simulation of the piezo driver with the non-linear piezo capacitance.

The output voltage, VN(PIEZO), does not show the same sinusoidal waveform as the input voltage does. This is caused by the non-linear behaviour of the piezo capacitance, since the piezo driver controls the charge. The charge inside the piezo element is therefore of importance for the control of the piezo element and not the voltage. Figure (5.6) shows the charge inside the piezo capacitor and the sense capacitor.

Fig. 5.5 Transient simulation of output signal with non-linear piezo capacitance.

The charge inside the piezo describes a sinusoidal waveform which is similar to the input signal. Another fact is that the charge inside the piezo and the sense capacitors are equal despite the non-linear capacitance of the piezo element.

Fig 5.6 Simulation of the charge inside the piezo capacitor and sense capacitor

From this it can be seen that the charge control gives a correct measure for the charge inside the piezo element. Therefore it can be stated that the charge is controlled in the correct way. The piezo driver can adapt to the non-linear behaviour of the piezo element.

For the next simulations a linear capacitor is used to have a linear dependence between the charge inside the piezo element and the voltage. This makes it easier to check the other requirements which the piezo driver has to satisfy and reduces the simulation time.

The next analyse shows the input and output signal at the output filter. The output signal is the voltage which is applied to the piezo element. This simulation made use of the controlled voltage source which replaced the output stage.
The simulation can be seen in figure (5.7). The simulation shows a sinus waveform with an amplitude of 60 Volt for the output signal, *VN(PIEZO)*. The piezo driver amplifies the 1 Volt input signal to a 60 Volt output signal. A maximum output voltage of 60 Volt and a gain of 60 where required for the piezo driver. These requirements are satisfied.

Fig. 5.7 simulation of the input, Piezo and feedback signal of the piezo driver.

When looking closer at the output signal, *VN(PIEZO)*, a small ripple can be seen. This is illustrated in figure (5.8). The ripple is about 180 mV at the output and at the feedback signal (*Vsense*) this is about 3 mV. This is in agreement with the equation (3.35) which was derived in section 3.2.4 to calculate the ripple on the output signal and feedback signal.
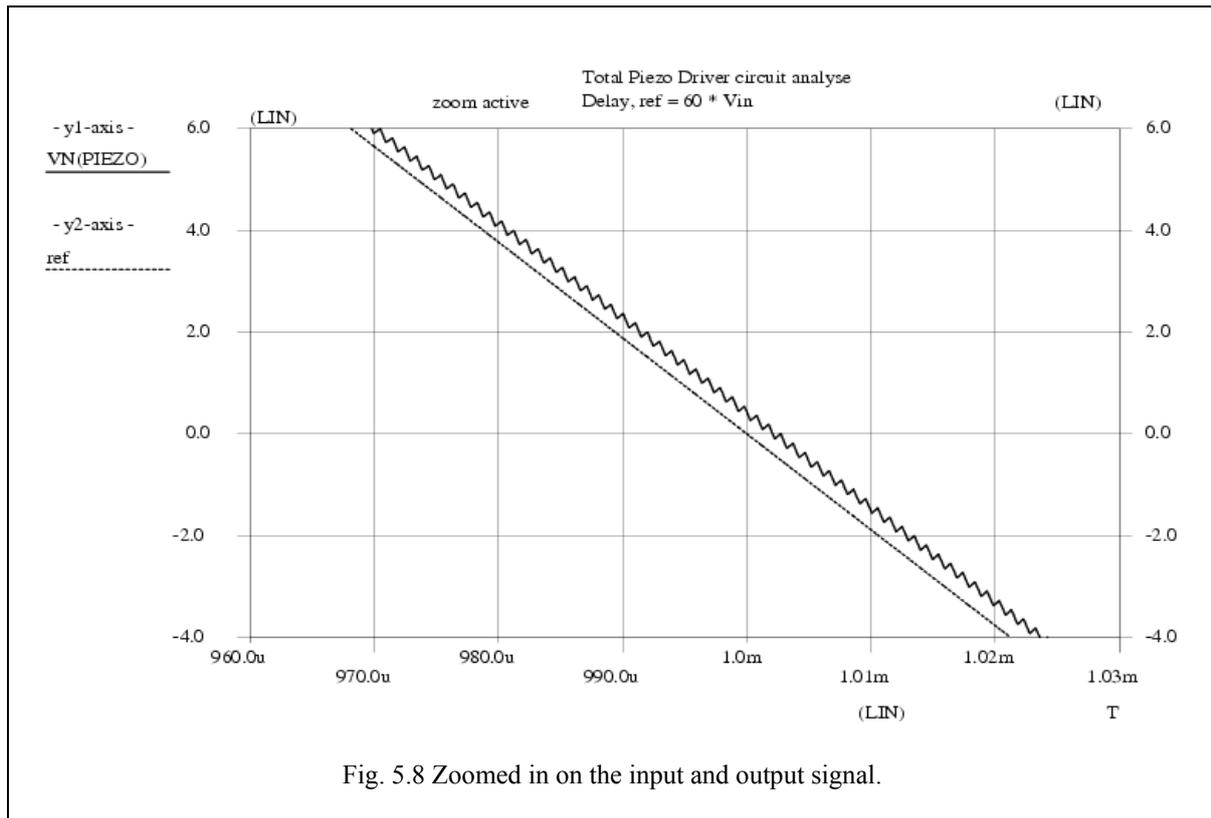
Fig. 5.8 Zoomed in on the input and output signal.

Using the formula to calculate the ripple on the feedback signal gives:

$$\hat{U}sense_{Ripple} = \frac{25\,\Omega}{60-1} \cdot 7.7\,mA = 3.22\,mV \tag{5.1}$$

Figure (5.8) does also show a delay of the output signal *VN(PIEZO)*. The input signal is used as reference to determine the time difference between the input and output signal. The input signal crosses the 0 Volt axes at 1 ms, the output signal does this 2.1 µs later. The delay is very small compared to the 2 ms period of the 500 Hz input signal. This delay is caused partly due to the processing time of the circuits and for the other part by the phase shift of the filter.

The delay can be interpreted as a phase shift of the used input signal. The delay gives a frequent depended phase shift and will give the maximum phase shift at the highest frequency. For a delay of 2.1 µs with a 500 Hz signal (period of 2 ms) the phase shift is:

$$Phase\ shift = \frac{2.1\,\mu s}{2\,ms} \cdot 360° = 0.37° \tag{5.2}$$

This is a small phase shift and satisfies the required maximum phase shift of 5˚. The AC simulation in the following section will show this as well.

The THD is calculated with an algorithm used in *PSTAR*. The algorithm, developed by Philips, determines the harmonic distortion in the output signal. The function *DISTORTT* contains the following calculations:

ADC=SUM(V0, Tp, Tl)/(Tl-Tp);

AACS=SUM(V0*SIN(2*Pi*FREQ*t),Tp, Tl)/(Tl-Tp);

AACC=SUM(V0*COS(2*Pi*FREQ*t), Tp, Tl)/(Tl-Tp);

AAC= 2*SQRT(AACS*AACS+AACC*AACC);

DISDIS=SUM((V0-2*AACS*SIN(2*Pi*FREQ*t)-
        2*AACC*COS(2*Pi*FREQ*t)-ADC)**2,Tp, Tl)/(Tl-Tp);

DISTORTT=SQRT(2*DISDIS)/AAC*100;

The function calculates the distortion of the signal *V0*. The starting time of the calculation is defined by *Tp* and the stop time by *Tl*. *FREQ* stands for the fundamental frequency of the signal *V0*.

The THD of the piezo driver design is calculated using the alternative circuit where the gate driver is replaced by the controlled voltage source. This circuit configuration obtained a THD of 0.084% which is quite good.
The THD is mainly caused by the switching of the output stage. The controlled voltage source is quite an ideal component so it is likely that the output stage (gate driver and output transistors) will produce more distortion. Simulations to calculate the THD of the total circuit design with output stage are still running and can therefore not be taken along in this report.

The piezo driver dissipation is calculated by measuring the power provided by the supply sources. The supplies are divided into the low-voltage and high-voltage sources. The power is calculated with the help of *PSTAR*. The dissipation is calculated over one complete period of the input signal. The same input signal with 1 Volt amplitude and 500 Hz is used for this simulation. The power delivered by supply source is derived with the use of equation (5.3)

$$P_{\sup ply} = \frac{1}{T_{sig}} \cdot \int_0^T i_{\sup ply}(t) \cdot V_{\sup ply} dt \tag{5.3}$$

The low-voltage supply sources are; the 2.5 V source, -2.5 V source and the two current mirrors of 50 μA and 25 μA. The total provided power of these sources is 9.8 mW.
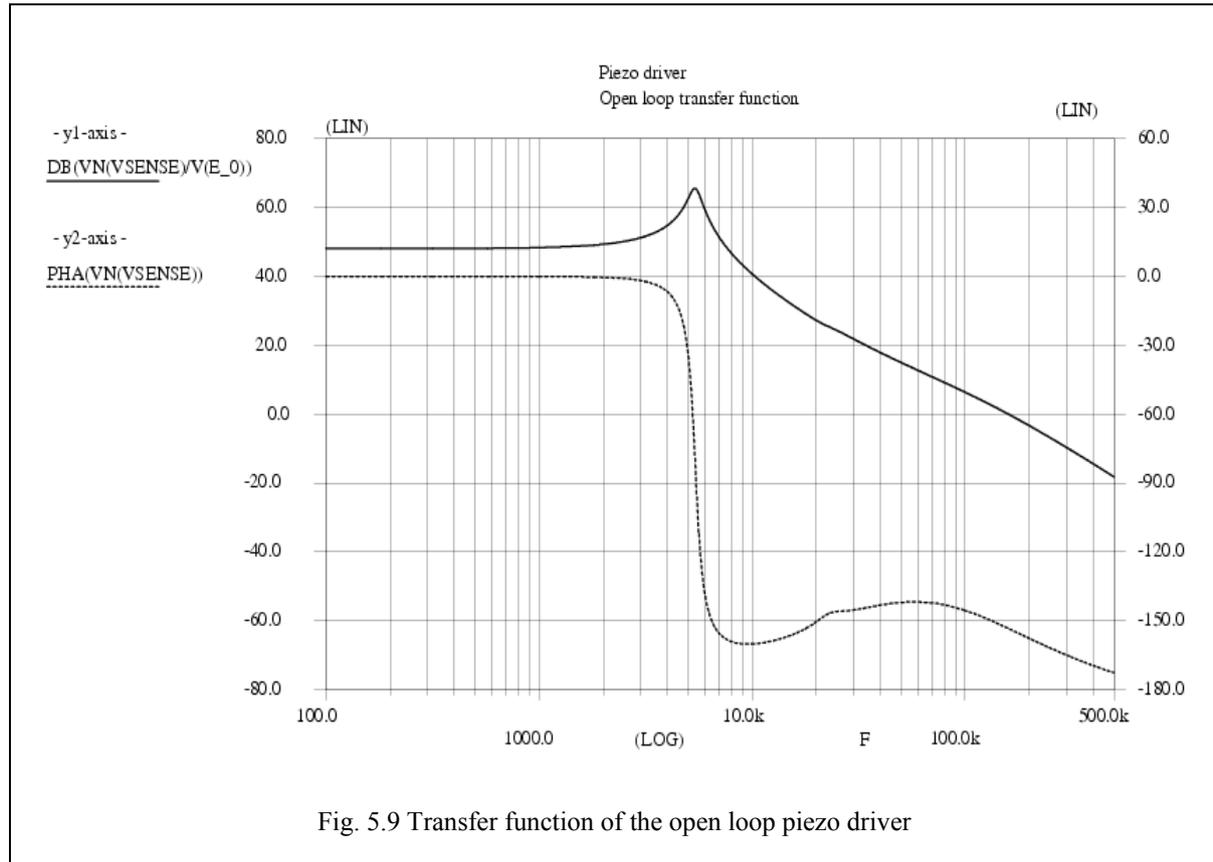The high-voltage supply sources are; the 48 V, 60 V, -48 V and -60 V source. These delivered a total power of 2.24 W.
The total power dissipation for the piezo driver is therefore 2.25 W. This is more than the approximated dissipation which was calculated in chapter three, though still low.

5.2 AC analyse

The PWM and output stage do also form a problem for the AC simulations. These simulation can not be done because of the switching properties of the PWM and output stage. The AC simulations use therefore a controlled voltage source to replace the PWM and output stage. This voltage source models the gain of the PWM and output stage which is 60.

The AC simulations are executed to check the stability and the phase shift of the piezo driver. The first AC simulation of the piezo driver is done with open loop and with the values of table (5.2) for the piezo model. Figure (5.9) shows the transfer function of the piezo driver.

Fig. 5.9 Transfer function of the open loop piezo driver

The feedback signal (*Vsense*) is used as the output signal and *V(E_0)* is the input signal. The phase shows a nice flat curve for the low frequencies. The phase shift at 500 Hz is approximately 0.4°, this was already showed in the previous section.
In chapter four the circuit design was tuned to ensure stability. As can be seen in figure (5.9) the phase shift is 151° at 0 dB. For this situation the system is stable.

However the piezo element can have a minimum and maximum capacitance of respectively 50 nF and 500 nF. The series resistor (*Rs*, fig 2.5) has been assumed with a minimum and maximum value of respectively 5 Ω and 50 Ω. Using these values for the piezo model gave the following results, see figure (5.10).

Fig. 5.10 AC simulation with min and max value for the piezo model.

In figure (5.10) the open-loop transfer function of the piezo driver is shown with the use of the 500 nF and 50 nF. The *VN(VFB_500nF)* and *VN(VFB_50nF)* are the feedback signals where respectively the maximum and minimum piezo capacitance have been used.
The simulation of the maximum piezo capacitance was done with the 50 Ω series resistor to show the maximum condition. The phase shift stays for this situation below 1° at 500 Hz. The phase shift at 0 dB is close to 150° giving a stable situation for the piezo driver.

However this is a different story for the minimum values of the piezo capacitance and series resistor. When 50 nF and 5 Ω are used for the piezo element the piezo driver becomes instable. For the simulation a series resistor of 35 Ω is used to show that the piezo driver is on the edge of instability, see figure (5.10). At 0 dB the phase shift is 174°. For lower values of the series resistor the system becomes instable.

There are two solutions for this problem. The first is to tune the circuit of the piezo driver so that the phase starts shifting at a higher frequency. Tuning does however mean that the circuits or/and component values have to be altered.
The other solution is to place a resistor in series with the piezo element. This brings the phase shift after the filters resonance frequency faster back 90° phase shift. The total phase shift, of the piezo driver circuits and the filter together, can be kept lower than 180° at 0 dB in this way. Placing a resistor in series with the piezo element does however increase the dissipation.

5.3 Summary simulations and tests

The simulated and calculated values of the piezo driver system are given below.

- Gain of 60.
- Maximum output voltage of ±60 Volt.
- Output signal delay of 2.1 µs.
- Phase shift @ 500 Hz of 0.4˚.
- THD[*] of 0.08%.
- Power dissipation of 2.25 Watt.

(*, measured with the adjusted piezo driver circuit.)

6. Conclusion and recommendations

The conclusion of this thesis is presented in this chapter. Beside the conclusion some recommendations are made in this section.

6.1 Conclusion

The main goal of this assignment was to design a system which can drive piezo-panels used for the ANC system of TNO. The main conclusion is that a circuit design is made which functions within the specified requirements. The three design stages in this project contributed all to the final result. The conclusion from these parts is discussed in the following.

The first stage of the project showed that piezoelectric material possesses unwanted electric behaviour, hysteresis and resonance. A model has been formed to predict and simulate the electric behaviour of the piezo-panel.
The hysteresis behaviour is cancelled by driving the piezo element with charge instead of voltage. The piezo driver is for this reason equipped with a charge control circuit which enables the system to control the charge inside the piezo-patch.
Further study of the piezoelectric material showed that the resonance frequencies start above the signal bandwidth. The study also showed that the resonance behaviour can be neglected at high frequencies. The output signal is not influenced by the piezoelectric resonances.

The second stage involved the functional design of the piezo driver. The piezo driver operates as an amplifier to provide the maximum output voltage of ±60 Volt. This output voltage is sufficient to fully drive the piezo-panel.
Research of different topologies showed that a class-D amplifier is best used as the main function of the piezo driver. This topology can realize low power dissipation while having a low distortion of the output signal. Simulation of the system calculated a dissipation of 2.25 W.
The class-D design is adjusted to cope with the hysteresis and resoance behaviour of the piezo element.

The pulse modulator is realised with a PWM scheme which uses a triangular waveform as reference signal. A triangle waveform gives the best results for PWM concerning EMI. The amplitude of the triangle is equal to the maximum input voltage of 1 Volt. This gives a gain of 60 for the piezo driver.
The high frequency (1 MHZ) for the triangular waveform provides a solution for the resonance behaviour of the piezo element. The piezo driver is not influenced by the electric resonance of the piezo element.

The filter is adjusted to the piezo-panels. The panel is incorporated into the *LC* filter design. Replacing the capacitor of the *LC* filter with the piezo element reduces the number of components needed on the plate. It also reduces the output current and thus reduces the dissipation of the piezo driver.
The maximum available inductance for the coil which can be placed on the panel is 3.9 mH. The bandwidth of the piezo driver is therefore between approximately 3.6 kHz and 11.4 kHz for the piezo capacitance of 500 nF and 50 nF respectively.

The filter uses the maximum available value of the coil for the filter design. The fixed value of the inductor makes it possible to determine the maximum ripple on the output signal for the given range of the piezo-patches.

After the filter feedback is applied. The feedback contains a charge control circuit to control the charge inside the piezo element. The control circuit consists of a capacitor and a resistor which are in series with the piezo element. The capacitor is used to determine the charge inside the piezo element and has to have a capacitance 59 times large than the piezo element. The resistor provides a stable operating situation for the piezo driver by reducing the phase shift of the feedback signal. The resistor has to be 59 times smaller than the resistance of the piezo-panel. Simulation shows that the charge control functions correctly.
The loop amplifier in the feedback is chosen at 250. This gain is low enough to ensure that the ripple on the feedback signal does not cause the piezo drivers output stage to switch unnecessary.

The main piezo driver circuits are designed in *Cadence* and can be integrated on chip. The technology used for the IC design is A-BCD. High voltage (e.g. ±60V) and low voltage circuits are realised on the same chip.
The inductor of the *LC* filter and the two charge control components are placed outside the IC. The number of components needed for the system is very small, in total four. The physical dimensions of piezo driver system are small. The height of an IC is less than 6 mm, which is the maximum available height for the piezo driver.

The designed circuits are; input buffer, subtractor, loop amplifier, PWM modulator and gate driver. All these circuits are simulated with *Pstar* and showed good results.

The piezo design is tested for all specifications. Not all simulations could be done with the complete piezo circuit because of the long simulation time. The simulation time is reduced by using a simplified output stage for certain simulations.
All requirements are satisfied except at one point. The minimum piezo capacitance and the minimum assumed piezo resistance cause instability of the system. This can however be solved by tuning the phase characteristic of the piezo circuits or/and placing extra resistance in series with the piezo element.

6.2 Recommendations

The simulations showed that the piezo driver satisfies the requirements. However some additional research and circuit design can improve the piezo driver.

- To test the complete circuit the THD calculation and charge control simulation should be done with the whole piezo driver design. The tests are now done with a controlled voltage source which replaces the piezo driver output stage.

- The mathematical model formed in this thesis can be improved by incorporating the energy losses of the piezoelectric material. The piezo model utilized in this project makes use of a resistor which is extracted from an impedance measurement. The piezo model has more value when the energy losses can be predicted with the use of the material constants.

- Another improvement for the model can be made by incorporating the stiffness and absorption of the panel. With this the model is also able to predict the height and width of the resonance peaks.

- The DC voltage on the sense capacitor of the charge control should be controlled. Offset currents can cause a DC voltage on the sense capacitor. This can be helped by placing a large resistor parallel to the sense capacitor. Another solution can be applying feedback which controls / adjusts the DC value.

- The minimum capacitance and minimum series resistance of the piezo element can cause the piezo driver to become instable. The piezo driver should be better tuned to provide less phase shift so that the system is also stable in this situation. If stability is guaranteed adding of extra series resistance to the piezo element won't be necessary.

- The complete chip design is not finished. For example the power supply and circuit protection functions still have to be designed. The complete chip layout has to be done as well.

- The designed circuits are not very robust. Deviation in the transistor sizes can cause offset voltages etc. This can influence the performance of the piezo driver.
  The circuits should have some protection or automatic adjustment to mismatch and size difference.

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Appendix I: Mechanical material constants.

Stress

In physics, stress is a measure of the internal distribution of force per unit area within a body that balances and reacts to the loads applied to it.. Simplifying assumptions are often used to represent stress as a vector for engineering calculations. The stress tensor σ_{ij} is defined by the equation (I.1):

$$dF_i = \sum_{j=1}^{3} \sigma_{ij}\, dA_j$$

(I.1)

where $[dF_1, dF_2, dF_3]$ is the force on a small area element $[dA_1, dA_2, dA_3]$ where the subscripts 1,2,3 refer to the x,y, and z axes respectively and the area vector is a vector perpendicular to the area element, with length equal to the area of the element.

Strain

Strain is the geometrical expression of deformation caused by the action of stress on a physical body. Strain therefore expresses itself as a change in size and/or shape. In the case of geological action of the earth, if the release of stress through strain in rocks is sufficiently large, earthquakes may occur.
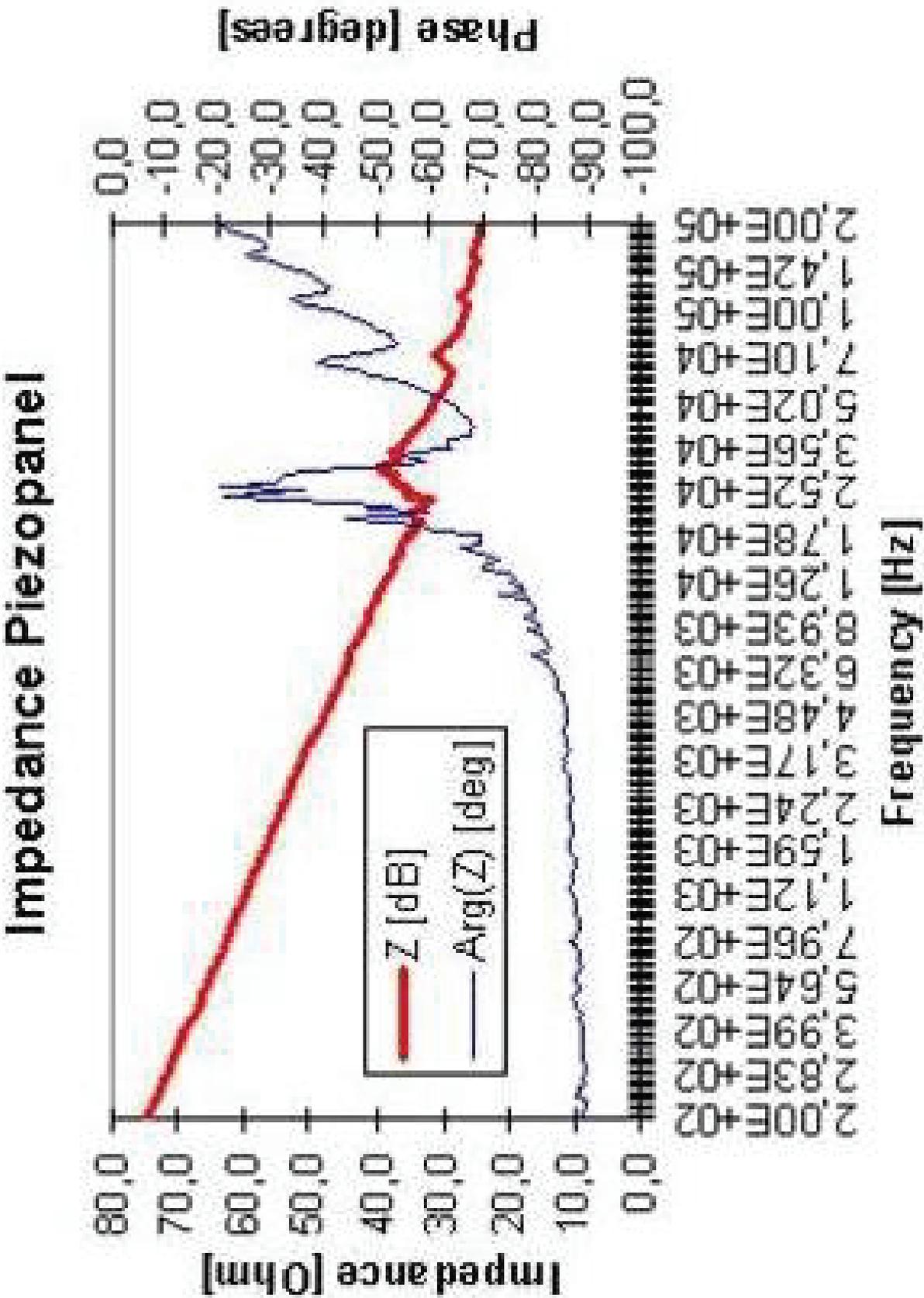
Young's modulus

In solid mechanics, Young's Modulus (also known as the Young Modulus, modulus of elasticity, elastic modulus or tensile modulus) is a measure of the stiffness of a given material. It is defined as the ratio, for small strains, of the rate of change of stress with strain. This can be experimentally determined from the slope of a stress-strain curve created during tensile tests conducted on a sample of the material. Young's modulus is named after Thomas Young the English physicist.

Poisson ratio

When a sample of material is stretched in one direction, it tends to get thinner in the other two directions. Poisson's ratio (*p*), named after Simeon Poisson, is a measure of this tendency. It is defined as the ratio of the contraction strain normal to the applied load divided by the extension strain in the direction of the applied load. For a perfectly incompressible material, the Poisson's ratio would be exactly 0.5. Most practical engineering materials have v between 0.0 and 0.5. Cork is close to 0.0, most steels are around 0.3, and rubber is almost 0.5. Some materials, mostly polymer foams, have a negative Poisson's ratio; if these exotic materials are stretched in one direction, they become thicker in perpendicular directions.
A Poisson's ratio greater than 0.5 does not make sense because at a certain strain the material would reach zero volume, and any further strain would give the material "negative volume".

Appendix II: TNO impedance measurement

Impedance Piezopanel

Appendix III: Maple sheet mathematical model

Determining the formula of the equivalent circuit of the piezo. The circuit consist of the piezo with a resistor (Rs) in series and a resistor (Rp) parallel to these. Formulating Zelec as the impedance of the equivalent circuit. Z1 is the piezo with the serie resistor.

```
> Zelec:=Z1*Rp/(Z1+Rp)*((b*cos(b)-C^2*sin(b))/(b*cos(b)));
```

$$Zelec := \frac{Z1\ Rp\ (b\cos(b) - C^2\sin(b))}{(Z1 + Rp)\ b\cos(b)}$$

For the impedance of the piezo with serie resistor we can use the following formula.
```
> Z1:=(1/(omega*Cp))+Rs;
```

$$Z1 := \frac{1}{w\ Cp} + Rs$$

```
> Cp:=A*Epsilon/h[p];
```

$$Cp := \frac{A\ \mathsf{E}}{h_p}$$

The following formula are needed to calculate the impedance:

```
> b:=2*h[host]*omega/(wave);
```

$$b := \frac{2\ h_{host}\ \mathsf{w}}{wave}$$

```
> wave:=1/sqrt(S[d]*rho[eq]);
```

$$wave := \frac{1}{\sqrt{S_d\ \mathsf{r}_{eq}}}$$

```
> S[eq]:=2*(1-v[p]^2)/Y[p]*k;
```

$$S_{eq} := \frac{2\ (1 - v_p^2)\ k}{Y_p}$$

```
> S[d]:=S[eq]*(1-C^2);
```

$$S_d := \frac{2\ (1 - v_p^2)\ k\ (1 - C^2)}{Y_p}$$

```
> k:=(12*Y[p]*h[p]*h[tot])/(24*X*(1-v[p]^2)+Y[p]*((h[host]+2*h[p])^3-h[host]^3));
```

$$k := \frac{12\ Y_p\ h_p\ h_{tot}}{24\ X\ (1 - v_p^2) + Y_p\ ((h_{host} + 2\ h_p)^3 - h_{host}^3)}$$

```
> X:=(Y[host]*h[host]^3)/(12*(1-v[host]^2));
```

$$X := \frac{Y_{host}\ h_{host}^3}{12 - 12\ v_{host}^2}$$

```
> rho[eq]:=1/h[tot]*(h[host]*rho[host]+h[p]*rho[p]);
```

$$\mathsf{r}_{eq} := \frac{h_{host}\ \mathsf{r}_{host} + h_p\ \mathsf{r}_p}{h_{tot}}$$

```
> Epsilon:=epsilon*(1-C^2);
```

$$\mathsf{E} := \mathsf{e}(1 - C^2)$$

```
> h[tot]:=h[p]+h[host];
```

$$h_{tot} := h_p + h_{host}$$

```
> A:=L[p]^2;
```

$$A := L_p{}^2$$

Filling in the constants

```
> Y[p]:=60.6e9;
```

$$Y_p := 6.06 \; 10^{10}$$

```
> Y[host]:=69.9e9;
```

$$Y_{host} := 6.99 \; 10^{10}$$

```
> C:=0.42;
```

$$C := 0.42$$

```
> v[p]:=0.33;
```

$$v_p := 0.33$$

```
> v[host]:=0.3;
```

$$v_{host} := 0.3$$

```
> h[host]:=4e-3;
```

$$h_{host} := 0.004$$

```
> h[p]:=0.1e-3;
```

$$h_p := 0.0001$$

```
> L[p]:=4e-2;
```

$$L_p := 0.04$$

```
> rho[p]:=7500;
```

$$\mathsf{r}_p := 7500$$

```
> rho[host]:=2700;
```

$$\mathsf{r}_{host} := 2700$$

```
> epsilon:=1900*8.85e-12;
```

$$\mathsf{e} := 1.681500 \; 10^{-8}$$

```
> omega:=f*2*Pi;
```

$$\mathsf{w} := 2 f \mathsf{p}$$
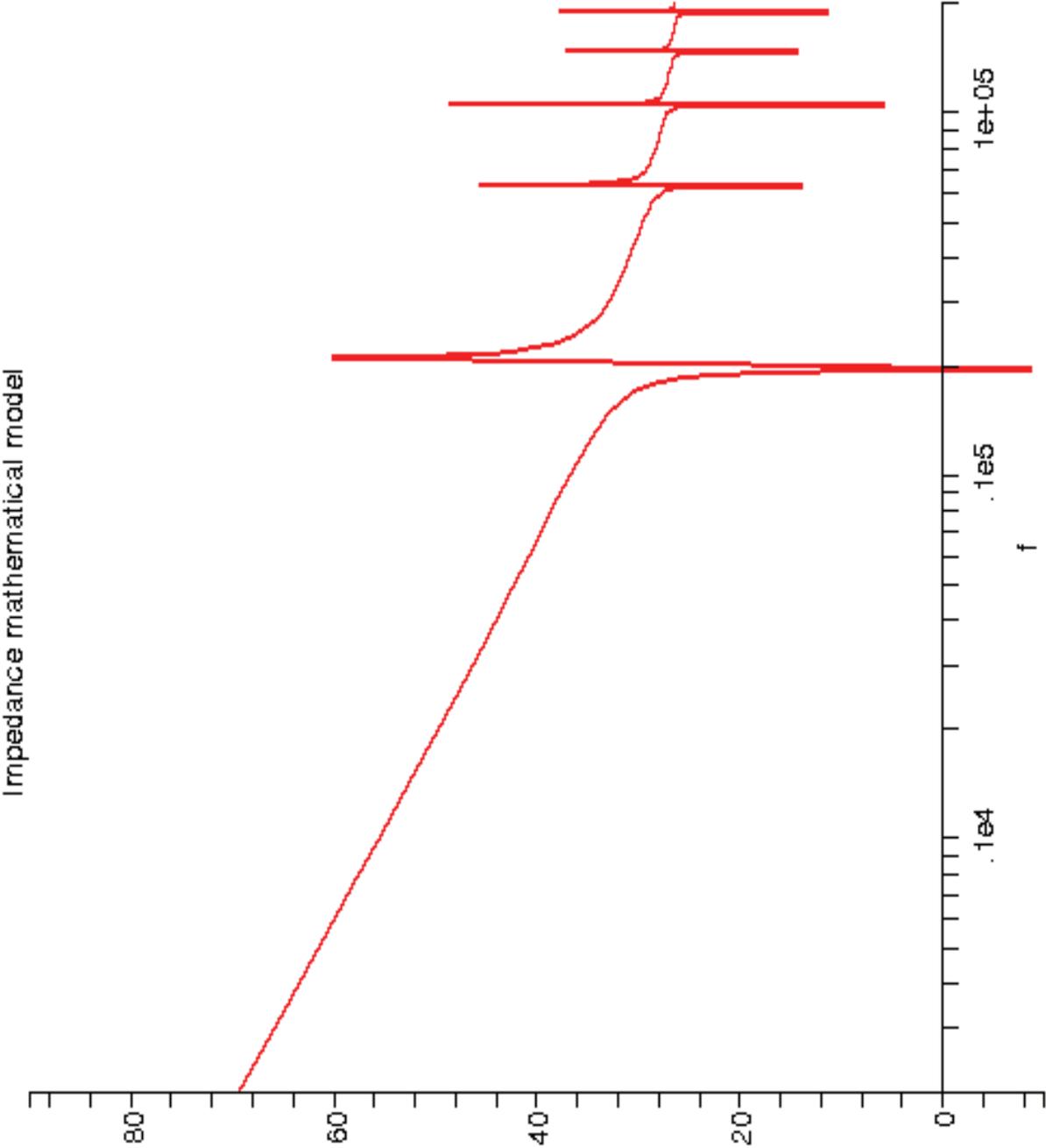
```
> Rs:=25;
```

$$Rs := 25$$

```
> Rp:=8e6;
```

$$Rp := 8 \; 10^6$$

Appendix IV: Mathematical model simulation

Impedance mathematical model

Appendix V: Equivalent circuit model simulation

- y1-axis -

DB(VN(OUT)/I(E_0))

- y2-axis -

phase - - - - -

Appendix VI: Dissipation calculations

Class-A

The class-A amplifier dissipation takes place in the NMOS and PMOS for the full sine wave. The power dissipated in the two transistors is calculated as follows:

$$Vout = A \cdot \sin(\omega t) \tag{V.1}$$

$$Iout = C \cdot \frac{dVout}{dt} = A \cdot C \cdot \omega \cdot \cos(\omega t) \tag{V.2}$$

The voltage over and current through the two transistors is:

$$V_{PMOS} = Vdd - Vout \tag{V.3}$$

$$V_{NMOS} = Vout - Vss \tag{V.4}$$

$$I_{PMOS} = I_{BIAS} + \frac{1}{2} \cdot Iout \tag{V.5}$$

$$I_{NMOS} = I_{BIAS} - \frac{1}{2} \cdot Iout \tag{V.6}$$

The total power dissipation of the Class-A is:

$$P_{PMOS} = \frac{1}{2\pi/\omega} \cdot \int_0^{2\pi/\omega} V_{PMOS} \cdot I_{PMOS} \; dt \tag{V.7}$$

$$= \frac{1}{2\pi/\omega} \cdot \int_0^{2\pi/\omega} \left(Vdd - A \cdot \sin(\omega t) \right) \cdot \left(I_{BIAS} + \tfrac{1}{2} A \cdot C \cdot \omega \cdot \cos(\omega t) \right) dt$$

$$= \frac{1}{2\pi/\omega} \cdot \int_0^{2\pi/\omega} Vdd \cdot I_{BIAS} + \tfrac{1}{2}Vdd \cdot C \cdot A \cdot \omega \cdot \cos(\omega t) - I_{BIAS} \cdot A \cdot \sin(\omega t) - \tfrac{1}{2} C \cdot A^2 \cdot \omega \cdot \sin(\omega t)\cos(\omega t) \, dt$$

$$= \frac{1}{2\pi/\omega} \cdot \left[Vdd \cdot I_{BIAS} \cdot t + \tfrac{1}{2}Vdd \cdot C \cdot A \cdot \sin(\omega t) + \frac{I_{BIAS} \cdot A \cdot \cos(\omega t)}{\omega} - \tfrac{1}{4} C \cdot A^2 \cdot \sin^2(\omega t) \right]_0^{2\pi/\omega}$$
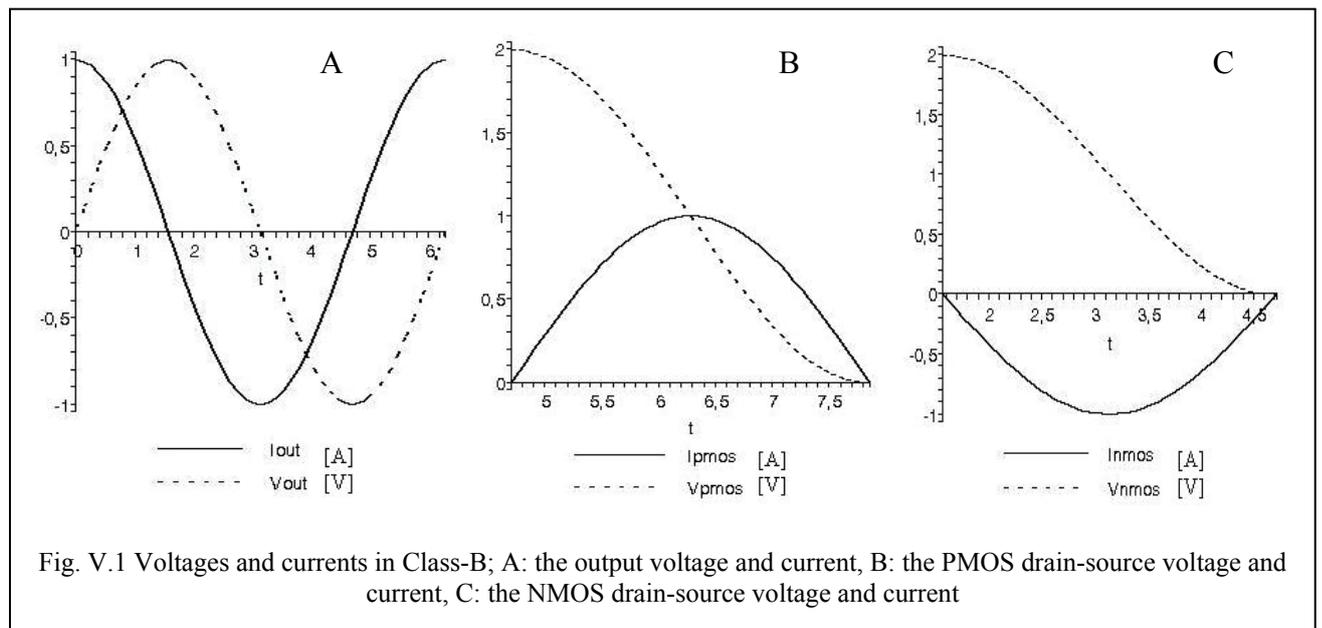
$$= I_{BIAS} \cdot Vdd$$

$$P_{NMOS} = \frac{1}{2\pi/\omega} \cdot \int_0^{2\pi/\omega} V_{NMOS} \cdot I_{NMOS} \; dt \qquad\qquad (V.8)$$

$$= \frac{1}{2\pi/\omega} \cdot \int_0^{2\pi/\omega} \left(A \cdot \sin(\omega t) - Vss\right) \cdot \left(I_{BIAS} - \tfrac{1}{2} A \cdot C \cdot \omega \cdot \cos(\omega t)\right) dt$$

$$= \frac{1}{2\pi/\omega} \cdot \int_0^{2\pi/\omega} -Vss \cdot I_{BIAS} + \tfrac{1}{2} Vss \cdot C \cdot A \cdot \omega \cdot \cos(\omega t) + I_{BIAS} \cdot A \cdot \sin(\omega t) - \tfrac{1}{2} C \cdot A^2 \cdot \omega \cdot \sin(\omega t)\cos(\omega t) \; dt$$

$$= \frac{1}{2\pi/\omega} \cdot \left[-Vss \cdot I_{BIAS} \cdot t + \tfrac{1}{2} Vss \cdot C \cdot A \cdot \sin(\omega t) - \frac{I_{BIAS} \cdot A \cdot \cos(\omega t)}{\omega} - \tfrac{1}{4} C \cdot A^2 \cdot \sin^2(\omega t) \right]_0^{2\pi/\omega}$$

$$= -I_{BIAS} \cdot Vss$$

With *Vss = -Vdd,* the total dissipation becomes:

$$P_{TOTAL} = P_{PMOS} + P_{NMOS} = 2 \cdot I_{BIAS} \cdot Vdd \qquad\qquad (V.9)$$

Class-B

The class-B amplifier dissipation takes place in the NMOS and PMOS for only a half of the sine wave. Because of the capacitive load the NMOS must conduct for the negative half of the current and the PMOS for the positive half of the current, showed in figure (V.1).

Fig. V.1 Voltages and currents in Class-B; A: the output voltage and current, B: the PMOS drain-source voltage and current, C: the NMOS drain-source voltage and current

The power dissipated in the two transistors is calculated using formula (V.1) for the output voltage and (V.2) for the output current. The voltage over the two transistors is the same as equation (V.3) and (V.4). The current through the two transistors is:

$$I_{PMOS} = Iout \tag{V.10}$$

$$I_{NMOS} = Iout \tag{V.11}$$

The power dissipation in the PMOS of the Class-B is:

$$
\begin{aligned}
P_{PMOS} &= \frac{1}{\frac{1}{2}\pi/\omega - \left(-\frac{1}{2}\pi/\omega\right)} \cdot \int_{-\pi/2\omega}^{\pi/2\omega} V_{PMOS} \cdot I_{PMOS}\, dt \\
&= \frac{1}{\pi/\omega} \cdot \int_{-\pi/2\omega}^{\pi/2\omega} C \cdot A \cdot \omega \cdot \cos(\omega t) \cdot (Vdd - A \cdot \sin(\omega t))\, dt \\
&= \frac{\omega}{\pi} \cdot \left[C \cdot A \cdot \left(Vdd \cdot \sin(\omega t) - \tfrac{1}{2} A \cdot \sin^2(\omega t)\right) \right]_{-\pi/2\omega}^{\pi/2\omega} \\
&= \frac{2\omega \cdot C \cdot A \cdot Vdd}{\pi}
\end{aligned}
\tag{V.12}
$$

The power dissipation in the NMOS of the class-B is:

$$
\begin{aligned}
P_{NMOS} &= \frac{1}{\frac{3}{2}\pi/\omega - \frac{1}{2}\pi/\omega} \cdot \int_{\pi/2\omega}^{3\pi/2\omega} V_{NMOS} \cdot I_{PMOS}\, dt \\
&= \frac{1}{\pi/\omega} \cdot \int_{\frac{1}{2}\pi/\omega}^{\frac{3}{2}\pi/\omega} C \cdot A \cdot \omega \cdot \cos(\omega t) \cdot (A \cdot \sin(\omega t) - Vss)\, dt \\
&= -\frac{\omega}{\pi} \cdot \left[C \cdot A \cdot \left(Vss \cdot \sin(\omega t) - \tfrac{1}{2} A \cdot \sin(\omega t)^2\right) \right]_{\pi/2\omega}^{3\pi/2\omega} \\
&= -\frac{2\omega \cdot C \cdot A \cdot Vss}{\pi}
\end{aligned}
\tag{V.13}
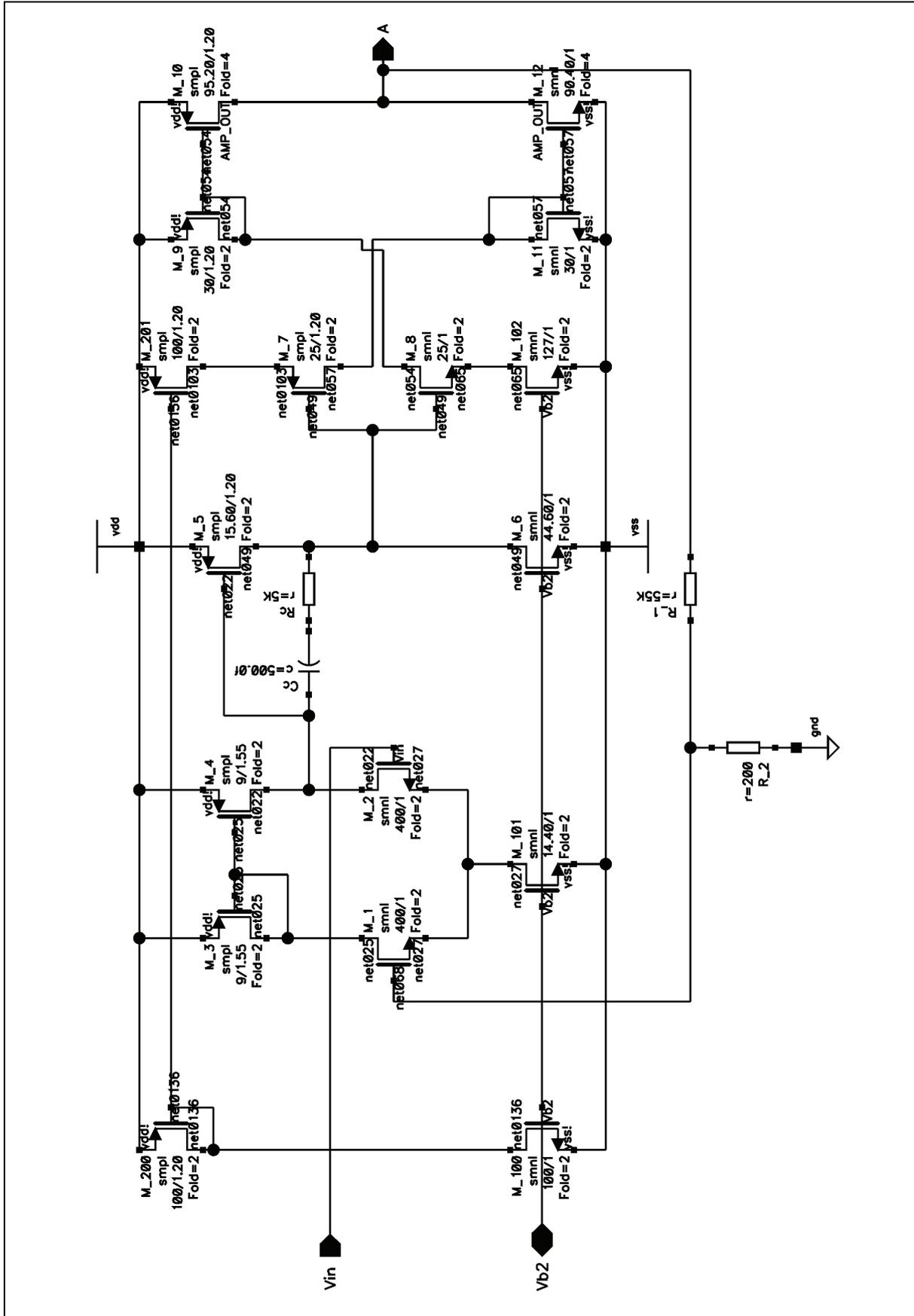$$

With *Vss = -Vdd,* the total dissipation becomes:

$$P_{TOTAL} = P_{PMOS} + P_{NMOS} = \frac{4\omega \cdot C \cdot A \cdot Vdd}{\pi} \tag{V.14}$$
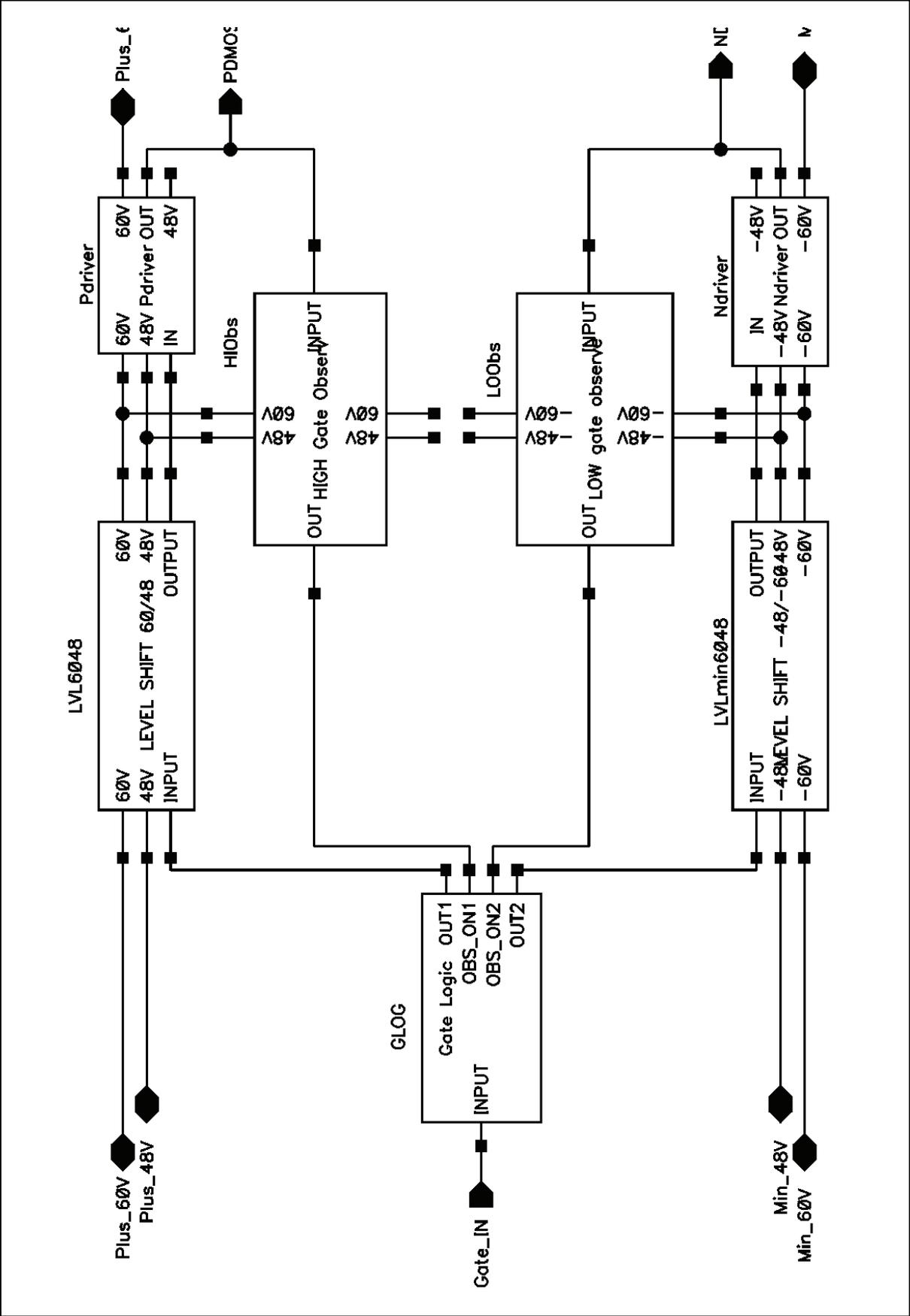
Class-AB

The class-AB amplifier functions almost the same as a class-B amplifier but the PMOS and NMOS are active between 180° and 360° of the input sine wave. This is done by biasing the circuit with a bias current. The total dissipation of a class-AB:

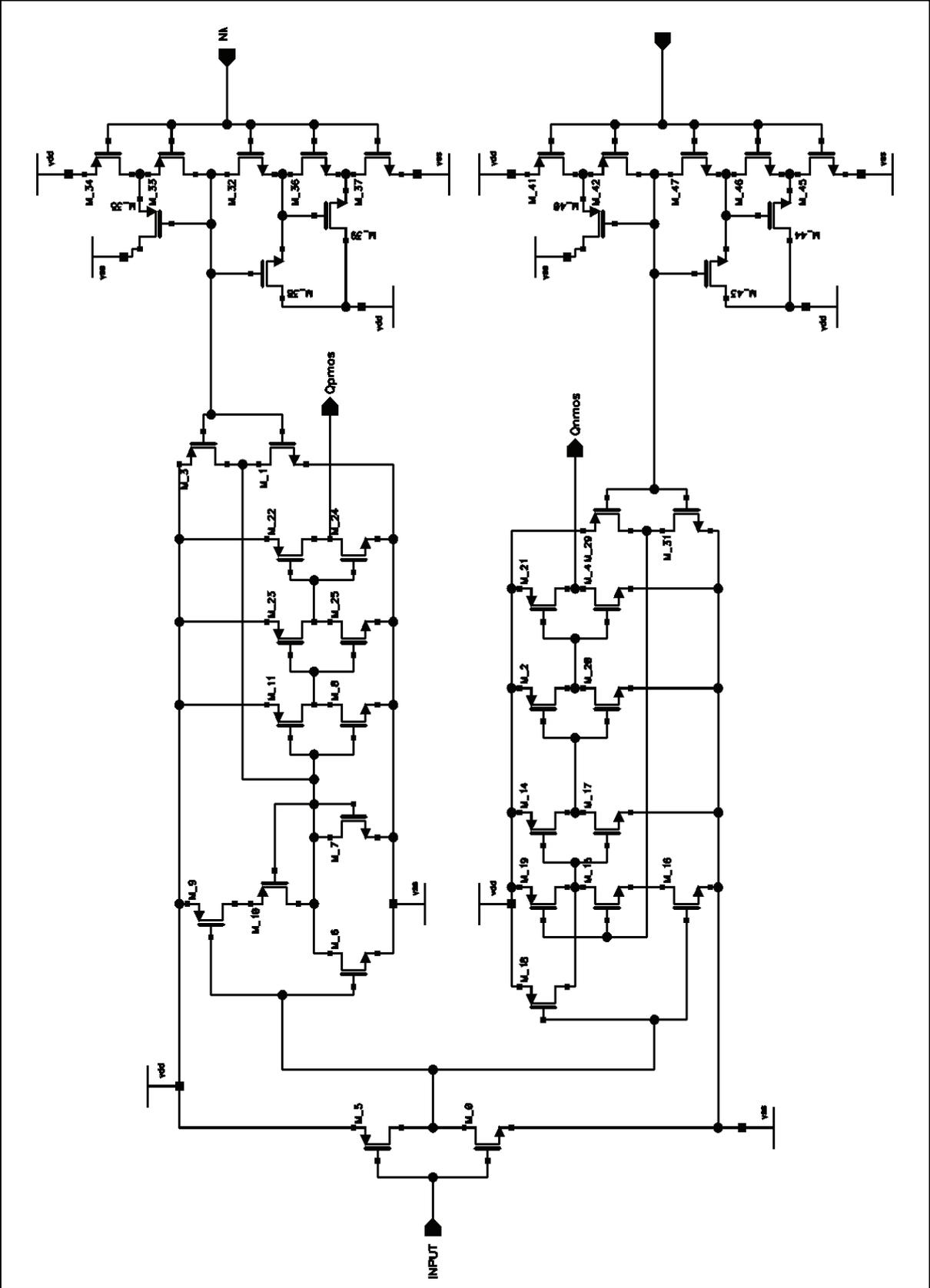$$P_{TOTAL} = \frac{4\omega \cdot C_{LOAD} \cdot A \cdot Vdd}{\pi} + 2 \cdot I_{BIAS} \cdot Vdd \tag{V.15}$$

Appendix VII: Buffer circuit design

Appendix VIII: Subtractor circuit design

Appendix X: Comparator circuit design

Appendix XII: Gate Driver circuit design

Appendix XIII: Gate logic circuit design

Appendix XV: Piezo Driver circuit design